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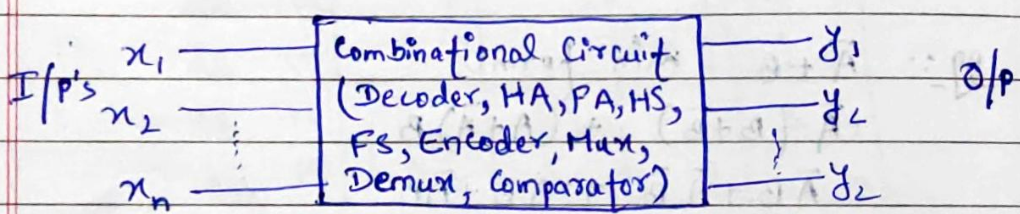
Unit 2

A decoder is a combinational circuit.
A decoder accepts a set of inputs that represents a binary number and activates only that output corresponding to the input number. All other outputs remain inactive.

There are 2^n possible input combinations. for each of these input combination only one output will be High (active) all other outputs are ~~low~~ LOW.

Combinational Circuit:-
Circuits in which output ~~only~~ depends only on the present input.



$n : 2^n$ (Format)

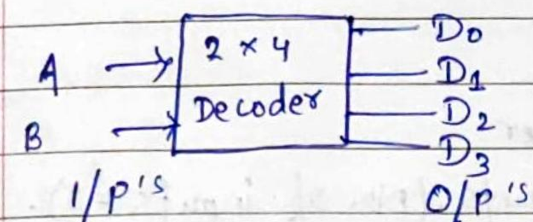
2 : 4

3 : 8

Types of Decoder

→ 2 to 4 line Decoder

A & B are the inputs (No. of inputs = 2).
No. of possible input combinations : 2^2 = 4
No. of Outputs : 2^2 = 4, they are indicated by D0, D1, D2, & D3
From the Truth Table it is clear that each output is "1" for only specific combination of inputs.



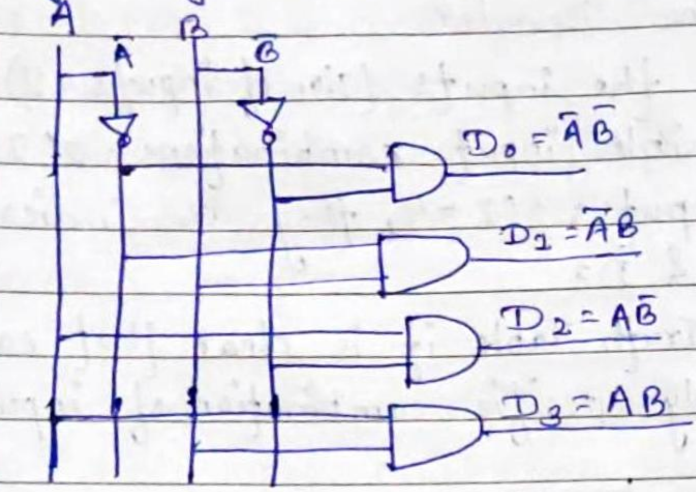
Truth Table

Inputs		Outputs			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Boolean Expression

$D_0 = \bar{A}\bar{B}$, $D_1 = \bar{A}B$, $D_2 = A\bar{B}$, $D_3 = AB$.

Logic diagram/Implementation

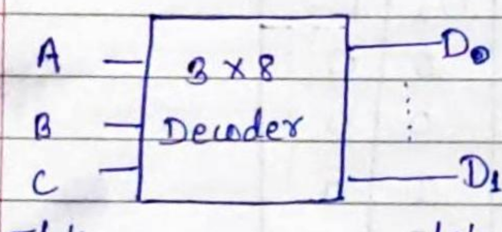


→ 3 to 8 line Decoder

A, B & C are the inputs. (No. of inputs = 3).

No. of possible input combinations : $2^3 = 8$

No. of outputs : $2^3 = 8$ they are indicated by D_0 to D_7

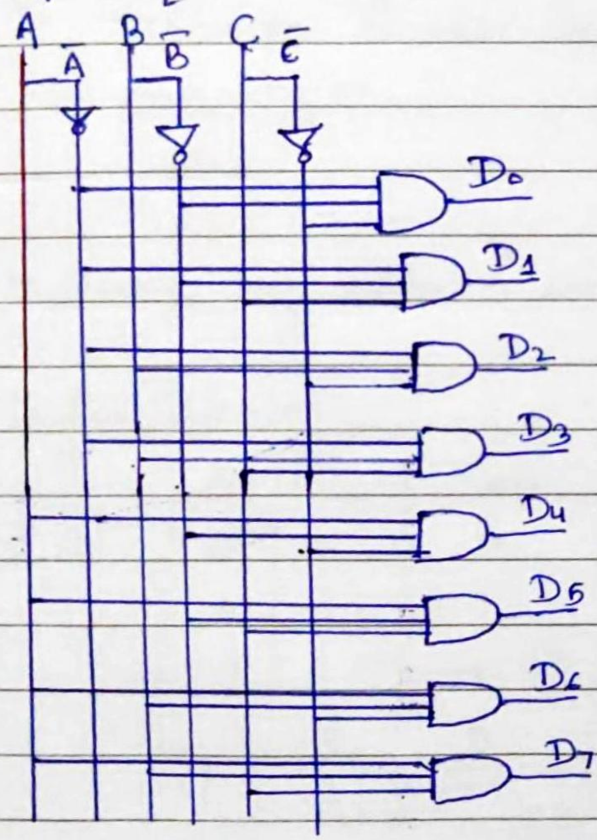


Truth Table

Input			Output								Boolean Exp.
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
0	0	0	1	0	0	0	0	0	0	0	$\bar{A}\bar{B}\bar{C}$
0	0	1	0	1	0	0	0	0	0	0	$\bar{A}\bar{B}C$

Inputs			Outputs								Boolean Exp
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
0	1	0	0	0	1	0	0	0	0	0	$\bar{A}B\bar{C}$
0	1	1	0	0	0	1	0	0	0	0	$\bar{A}BC$
1	0	0	0	0	0	0	1	0	0	0	$A\bar{B}\bar{C}$
1	0	1	0	0	0	0	0	1	0	0	$A\bar{B}C$
1	1	0	0	0	0	0	0	0	1	0	$AB\bar{C}$
1	1	1	0	0	0	0	0	0	0	1	ABC

Implementation



$\bar{G}_{2A}$	$\bar{G}_{2B}$	G_1	A	B	C	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
0	0	0	x	x	x	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1

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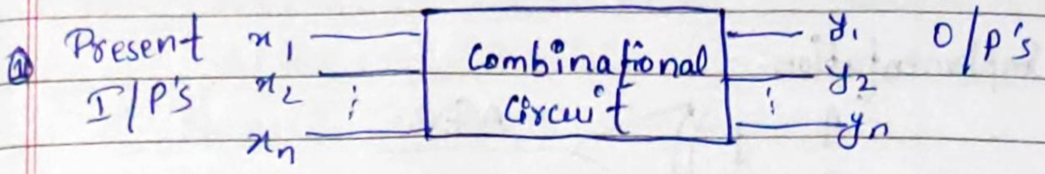
Combinational Circuit



② O/P depends only on present I/P's.
③ No feedback
④ No memory
⑤ No clock signal is applied here.
⑥ eg:- Half-adder, full-adder, half-subtractor, full- ~~subtrac~~ subtractor, encoder, decoder, mux, demux, comparator.

Half-adder

Q1 Implement half-adder & write it's truth table?

* Truth-Table :-

$2^n = 4$

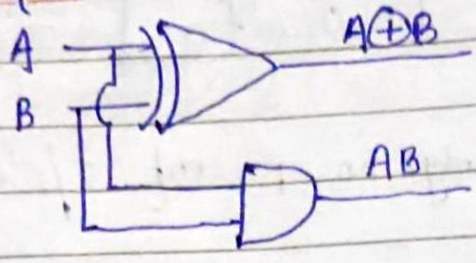
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Expression:-

Sum $= \bar{A}B + A\bar{B} = A \oplus B$

Carry = AB

Implementation:-



Q2. Implement full-adder, write its truth table.

* Truth-Table:-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression:-

Sum = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

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Boolean Expression:-

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$\bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$\bar{B}C + B\bar{C} = B \oplus C = x$$

$$\bar{B}\bar{C} + BC = \overline{B \oplus C} = \bar{x}$$

$$\bar{A}x + A\bar{x}$$

$$A \oplus x$$

$$(A \oplus B) \oplus C \;/\; A \oplus (B \oplus C)$$

EXOR:-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$Y = \bar{A}B + A\bar{B}$$
$$= A \oplus B$$

Exnor:-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

$$Y = \bar{A}\bar{B} + AB = \overline{A \oplus B} = A \odot B$$

$$Carry = \Sigma m(3, 5, 6, 7)$$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	1 (3)	2
A 1	4	1 (5)	1 (7)	1 (6)

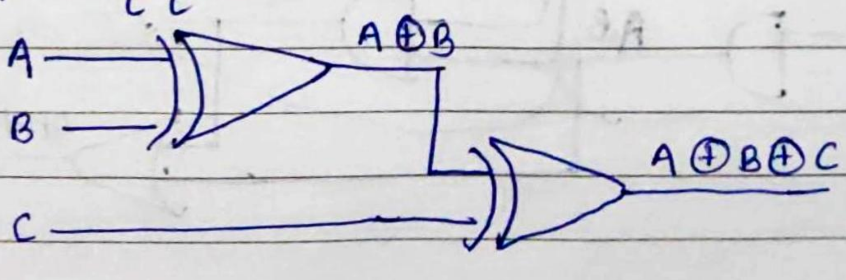
A	B	C
0	1	1
1	1	1
x	B	C

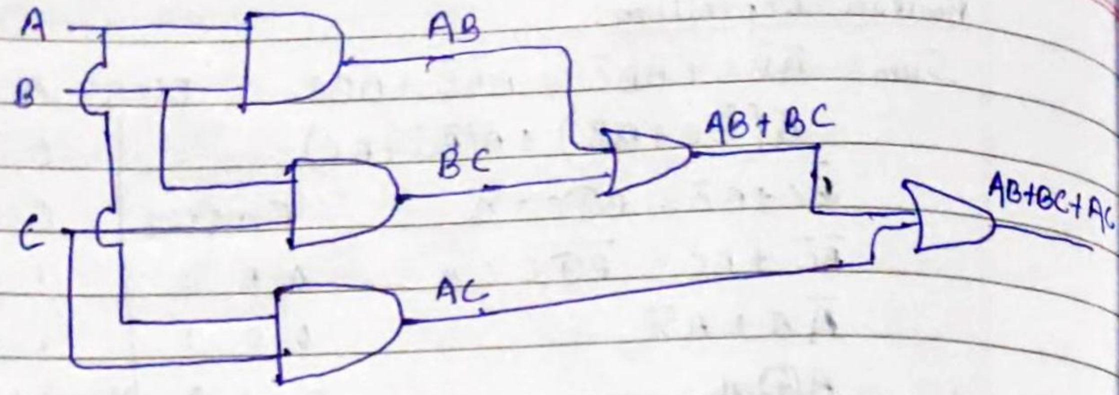
A	B	C
1	0	1
1	1	1
A	x	C

A	B	C
1	1	1
1	1	0
A	B	x

$$Carry = AB + BC + AC$$

Implementation:-





Q Implement full-adder using half-adder.

* $Sum = A \oplus B \oplus C$

$Carry = AB + BC + AC$

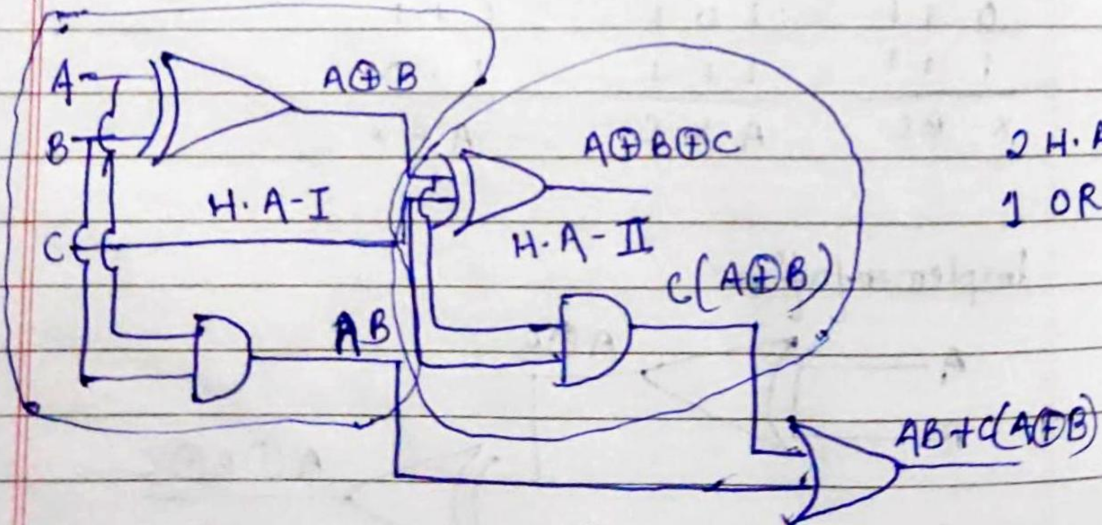
$= AB(C+\bar{C}) + (A+\bar{A})BC + A(B+\bar{B})C$

$= ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C$

$= ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$

$= AB(C+\bar{C}) + C(\bar{A}B + A\bar{B})$

$= AB + C(A \oplus B)$



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Multiplexer (combinational circuit)

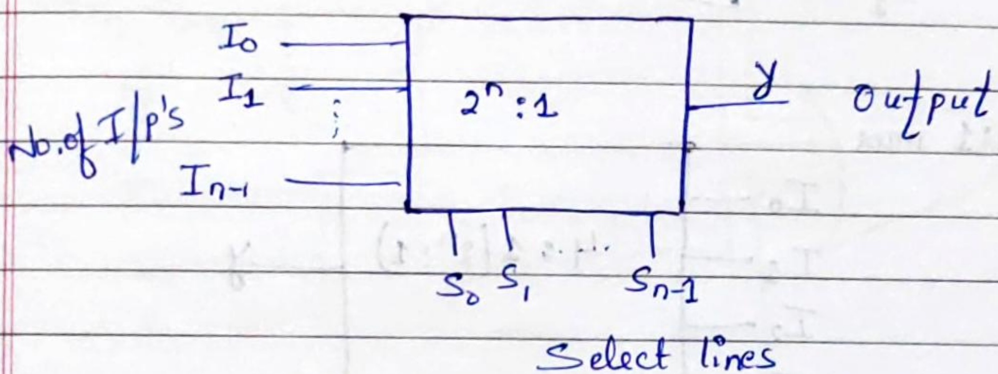
- ↳ Many to one circuit
- ↳ Many I/P's → Single O/P
- ↳ I/P - O/P relation :-

$2^n : 1$

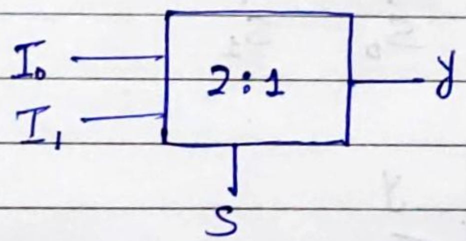
Total no. of inputs

n = no. of select lines.

Block diagram:-



* 2:1 mux



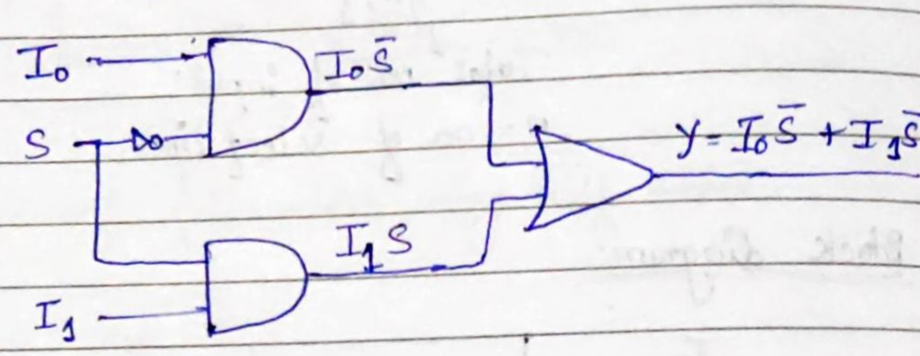
Truth-Table :-

S	Y
0	I_0
1	I_1

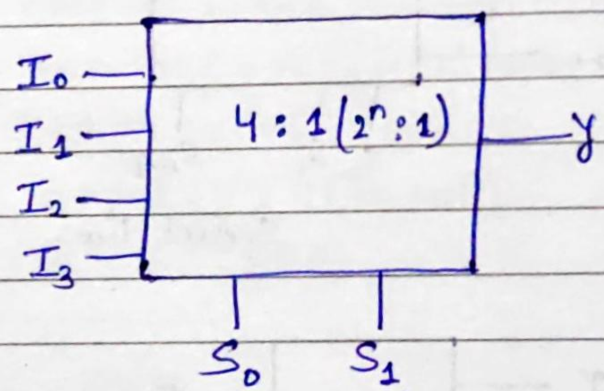
Boolean Expression:

$Y = I_0\bar{S} + I_1S$

Implementation :-



* 4:1 mux



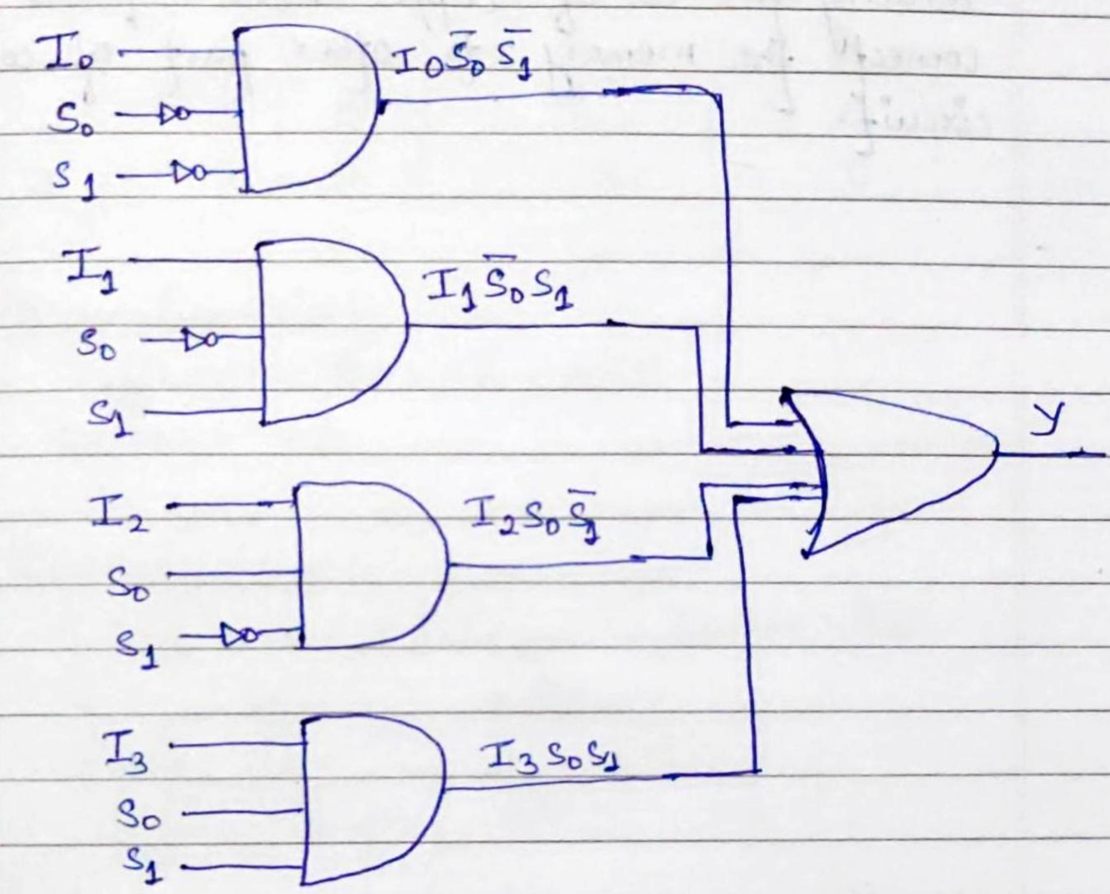
Truth-Table

S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Boolean Expression:-

$$y = I_0 \bar{S}_0 \bar{S}_1 + I_1 \bar{S}_0 S_1 + I_2 S_0 \bar{S}_1 + I_3 S_0 S_1$$

Implementation:-



↳ A multiplexer is known as data selector. It is a device that selects b/w ~~sel sevet~~ several analog or digital inputs and forward it to a single output line. It has select lines, used to select the input line to be sent to output ~~line~~.

NOTE: In decoder ~~e~~ input must be binary

Multiplexor are used to implement huge about of memory into the computer which helps by ~~reducin~~ reducing the no. of copper lines required to connect the memory to other part of computer circuit.

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Half - Subtractor

Truth-table:-

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

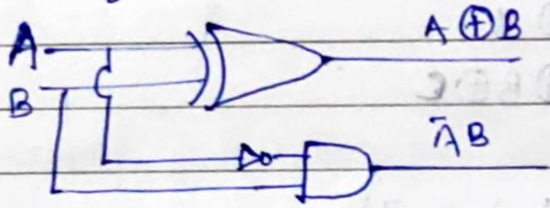
Boolean-Expression:-

Difference = $\bar{A}B + A\bar{B} = A \oplus B$

Borrow = $\bar{A}B$

Implementation:-

Difference = $A \oplus B$, Borrow = $\bar{A}B$



Full - Subtractor

A B C Difference Borrow

Full Subtractor **Truth table:-**

A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Boolean Expression:-

Difference $= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}x + A\bar{x}$

$= A \oplus x$

$= A \oplus B \oplus C$

Borrow $= \Sigma m(1,2,3,7)$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1 1	1 3	1 2
A 1	4	5	1 7	6

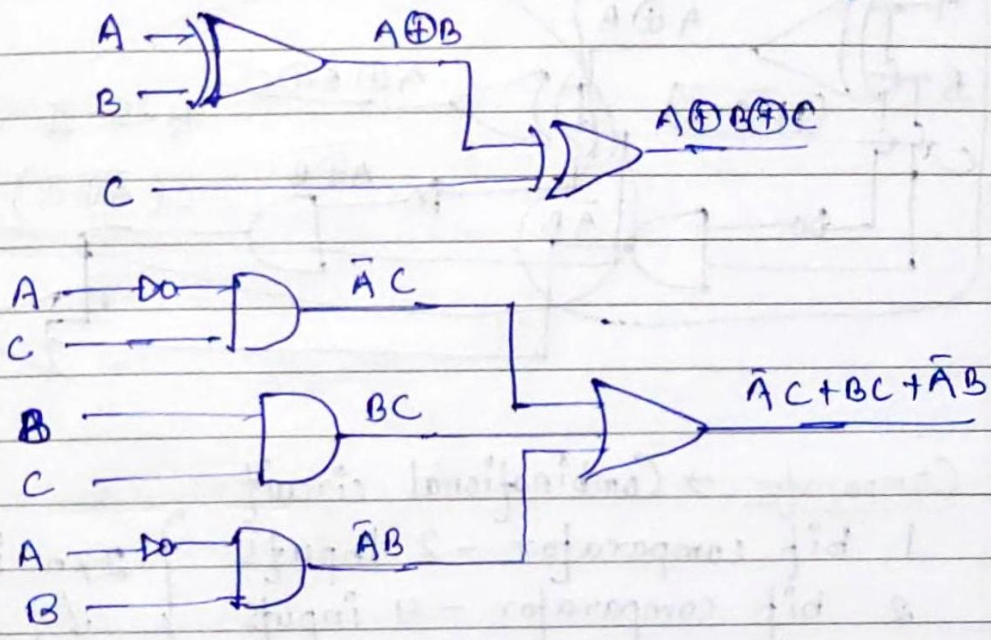
A B C	A B C	A B C
0 0 1	0 1 1	0 1 1
0 1 1	1 1 1	0 1 0
$\bar{A}$ x C	x B C	$\bar{A}$ B x

$\bar{A}B + BC + \bar{A}B$ = Borrow.

Implementation :-

Difference = $A \oplus B \oplus C$

Borrow: $\bar{A}B + BC + \bar{A}B$



Q Implement full-subtractor using half-subractor.

Difference = $A \oplus B \oplus C$

Borrow = $\bar{A}B + BC + \bar{A}C$

$= \bar{A}B(C+\bar{C}) + (\bar{A}+A)BC + \bar{A}(B+\bar{B})C$

$= \bar{A}BC + \bar{A}B\bar{C} + \bar{A}BC + ABC + \bar{A}BC + \bar{A}\bar{B}C$

$= \bar{A}BC + \bar{A}B\bar{C} + ABC + \bar{A}\bar{B}C$

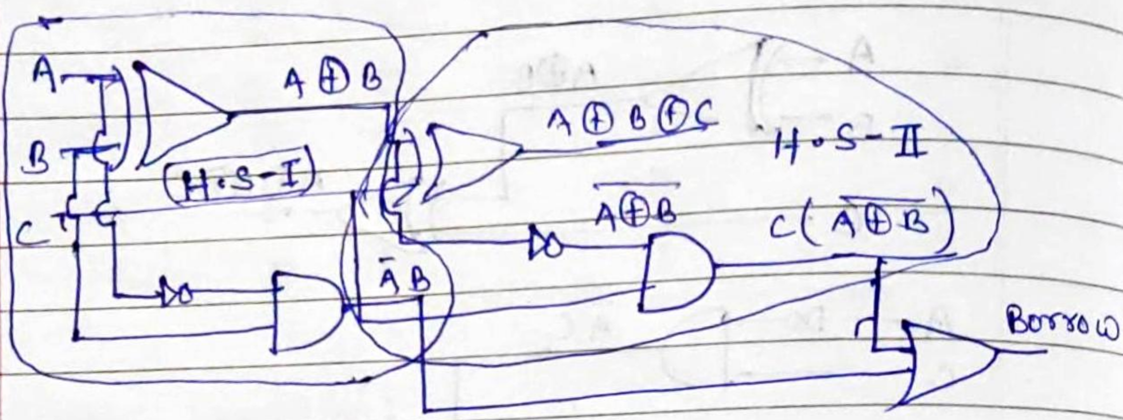
$= \bar{A}B(C+\bar{C}) + C(\bar{A}\bar{B} + AB)$

$= \bar{A}B + C(\overline{A \oplus B})$

Implementation:-

Difference $= A \oplus B \oplus C$

Borrow $= \bar{A}B + C(\overline{A \oplus B})$



Comparator → Combinational circuit

1 bit comparator - 2 inputs

2 bit comparator - 4 inputs

3 bit comparator - 6 inputs

} 2×n inputs → n: no. of bits

* 1-bit comparator Truth-table:-

A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

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* 1-bit Comparator :- 2 I/p's → 2×n (n: no. of bits)

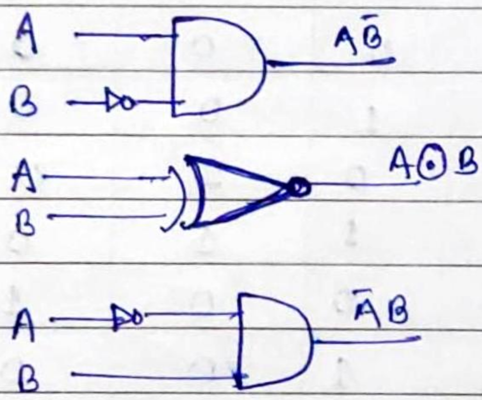
Boolean-Expression:-

$A > B \Rightarrow A\bar{B}$

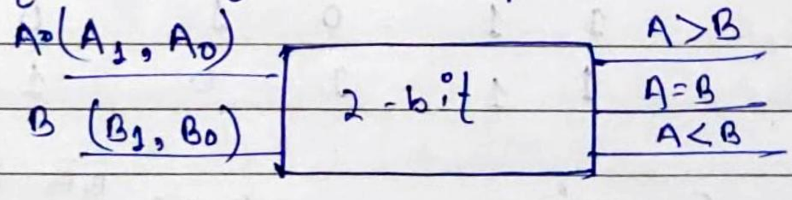
$A = B \Rightarrow \bar{A}\bar{B} + AB = \overline{A \oplus B}$

$A < B \Rightarrow \bar{A}B$

Implementation :-



* 2-bit Comparator :- 4 I/p's



Truth-table :-

A		B		A > B	A = B	A < B
A_1	A_0	B_1	B_0			
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Boolean Expression:-

$A > B = \Sigma m(4, 8, 9, 12, 13, 14)$

A_1A_0 \ B_1B_0	$\bar{B_1}\bar{B_0}$ 00	$\bar{B_1}B_0$ 01	B_1B_0 11	$B_1\bar{B_0}$ 10
$\bar{A_1}\bar{A_0}$ 00	0	1	3	2
$\bar{A_1}A_0$ 01	1 4	5	7	6
A_1A_0 11	1 12	1 13	15	1 14
$A_1\bar{A_0}$ 10	1 8	1 9	11	10

A_1	A_0	B_1	B_0
1	1	0	0
1	1	0	1
1	0	0	0
1	0	0	1
A_1	x	$\bar{B}_1$	x

A_1	A_0	B_1	B_0
0	1	0	0
1	1	0	0
x	A_0	$\bar{B}_1$	$\bar{B}_0$

A_1	A_0	B_1	B_0
1	1	0	0
1	1	1	0
A_1	A_0	x	$\bar{B}_0$

$A>B = A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_0A_1\bar{B}_0$

$A=B = \Sigma m(0,5,10,15)$

A_1A_0 \ B_1B_0	00	01	11	10
00	1 (0)	1	3	2
01	4	1 (5)	7	6
11	12	13	1 (15)	14
10	8	9	11	1 (10)

$A=B \Rightarrow \bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0\bar{B}_1B_0 + A_1A_0B_1B_0 + A_1\bar{A}_0B_1\bar{B}_0$

$= \bar{A}_1\bar{B}_1(\bar{A}_0\bar{B}_0 + A_0B_0) + A_1B_1(\bar{A}_0\bar{B}_0 + A_0B_0)$

~~$A<B = \Sigma m(1,2,3,6$~~, $(\bar{A}_1\bar{B}_1 + A_1B_1)(\bar{A}_0\bar{B}_0 + A_0B_0)$

$(A_1 \odot B_1)(A_0 \odot B_0)$

$A<B = \Sigma m(1,2,3,6,7,11)$

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1 (1)	1 (3)	1 (2)
01	4	5	1 (7)	1 (6)
11	12	13	15	14
10	8	9	1 (11)	10

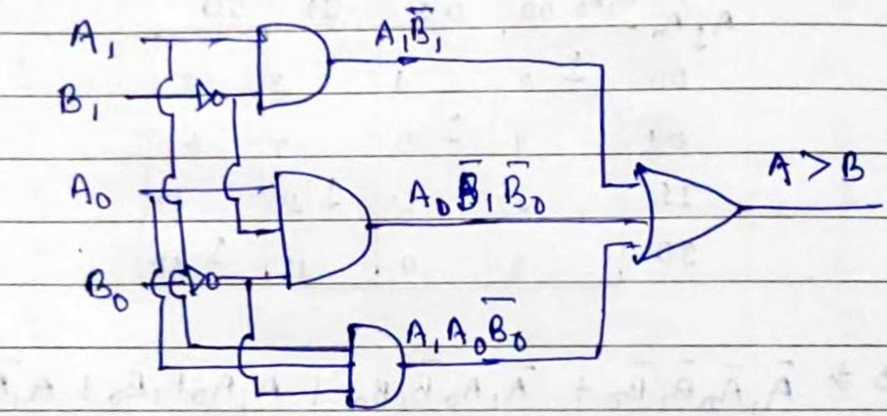
A_1	A_0	B_1	B_0
0	0	1	1
0	0	1	0
0	1	1	1
0	1	1	0
$\bar{A}_1$	x	B_1	x

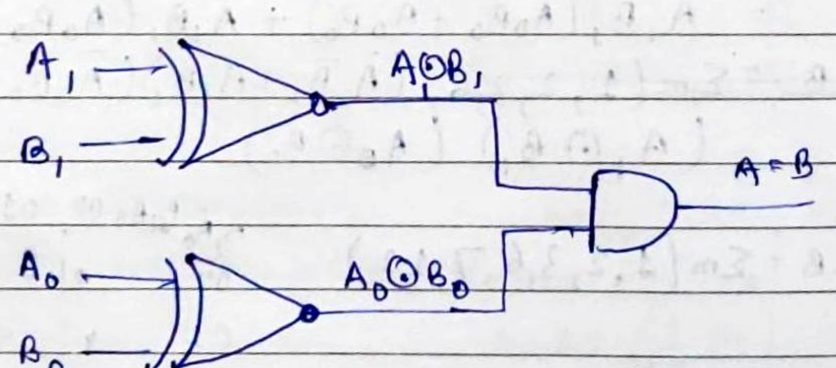
A_1	A_0	B_1	B_0
0	0	0	1
0	0	1	1
$\bar{A}_1$	$\bar{A}_0$	x	B_0

A_1	A_0	B_1	B_0
0	0	1	1
1	0	1	1
x	$\bar{A}_0$	B_1	B_0

$$A < B = \cancel{A_1 B_1}\ \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 B_1 B_0$$

Implementation:-





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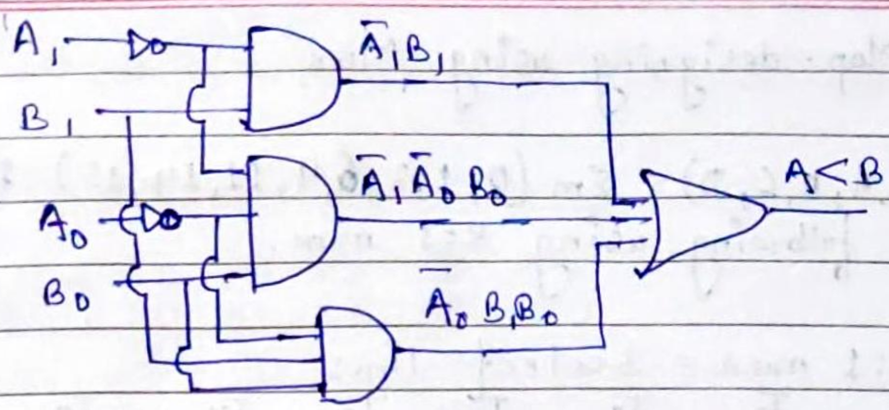

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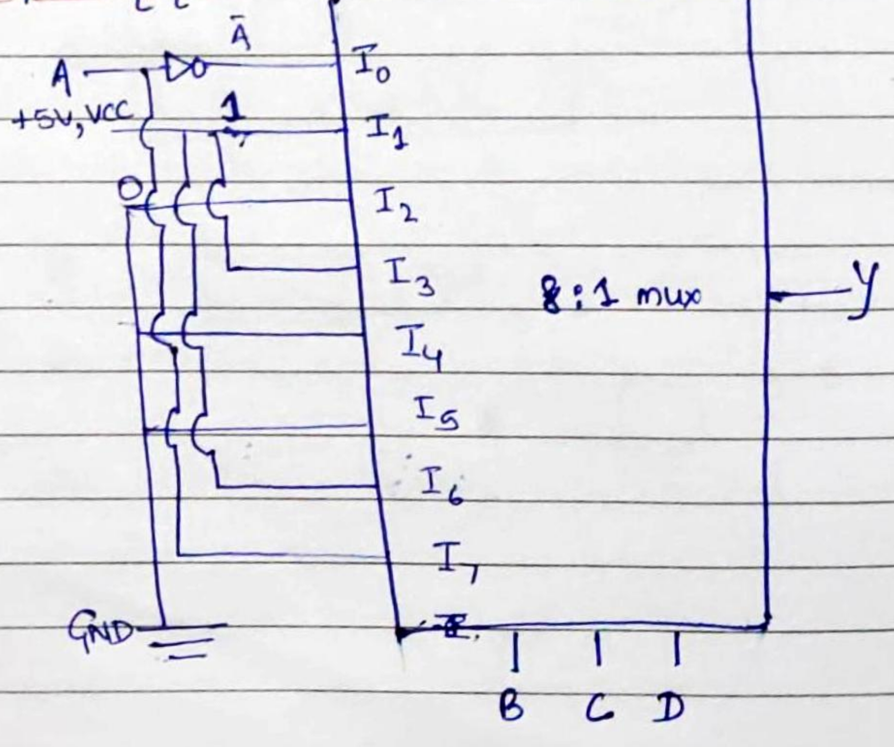
* K-Map designing using Mux

Q: $f(A,B,C,D) = \Sigma m(0,1,3,6,9,11,14,15)$ implement the following using 8:1 mux.

→ 8:1 mux = 3 select lines

A \ BCD	I_0 $\bar{B}\bar{C}\bar{D}$ 000	I_1 $\bar{B}\bar{C}D$ 001	I_2 $\bar{B}C\bar{D}$ 010	I_3 $\bar{B}CD$ 011	I_4 $B\bar{C}\bar{D}$ 100	I_5 $B\bar{C}D$ 101	I_6 $BC\bar{D}$ 110	I_7 BCD 111
$\bar{A}$ 0	0	1	2	3	4	5	6	7
A 1	8	9	10	11	12	13	14	15
	$\bar{A}$	$\bar{A}+A$ (1)	0	$\bar{A}+A$ (1)	0	0	$\bar{A}+A$ (1)	A

Implementation:-



Q $f\ \Sigma m\,(0, 1, 4, 7, 9, 11, 12, 14, 15)$ implement using 4:1 mux

→ 4:1 mux = 2 select lines

AB \ CD	$\bar C\bar D$ 00	$\bar C D$ 01	$C\bar D$ 10	CD 11
$\bar A\bar B$ 00	0	1	2	3
$\bar A B$ 01	4	5	6	7
$A\bar B$ 10	8	9	10	11
AB 11	12	13	14	15
	$\bar A\bar B+\bar AB+AB$	$\bar B$	AB	$\bar AB+A\bar B+AB$

$\bar AB + A$

$(A+\bar A)(A+B)$

$(A+B)$

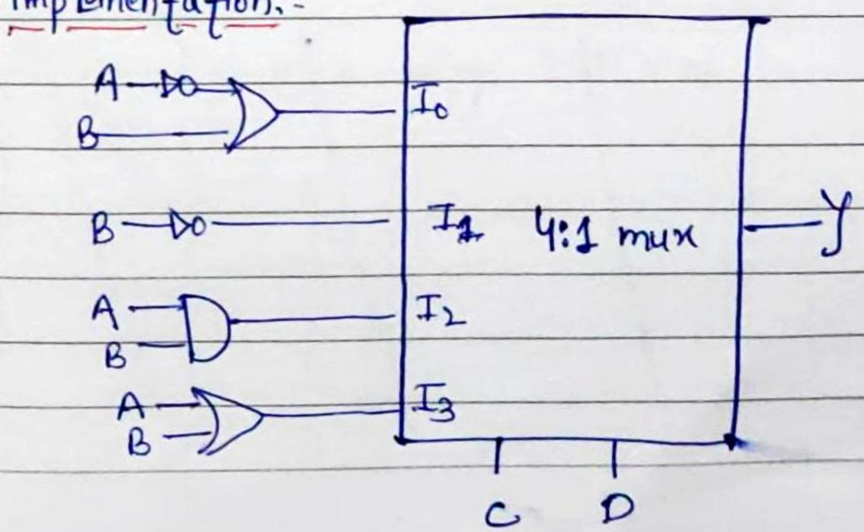
$\bar A\bar B+\bar AB+AB$

$\bar A + AB$

$(\bar A+A)(\bar A+B)$

$\bar A+B$

Implementation:-



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Q3 $\Sigma m(0,2,6,9,11,13,15)$ implement using 2:1 mux

ABC \ D	$\bar{D}$ 0	D 1
$\bar{A}\bar{B}\bar{C}$ 000	0	1
$\bar{A}\bar{B}C$ 001	2	3
$\bar{A}B\bar{C}$ 010	4	5
$\bar{A}BC$ 011	6	7
$A\bar{B}\bar{C}$ 100	8	9
$A\bar{B}C$ 101	10	11
$AB\bar{C}$ 110	12	13
ABC 111	14	15

$\bar{A}\bar{B}\bar{C}+\bar{A}\bar{B}C+\bar{A}BC$

$\bar{A}\bar{B}+\bar{A}BC$

$\bar{A}$

$A\bar{B}\bar{C}+A\bar{B}C+AB\bar{C}+ABC$

$A(\bar{B}\bar{C}+BC)+A(\bar{B}C+B\bar{C})$

$A(\bar{B}\bar{C}+BC)+$

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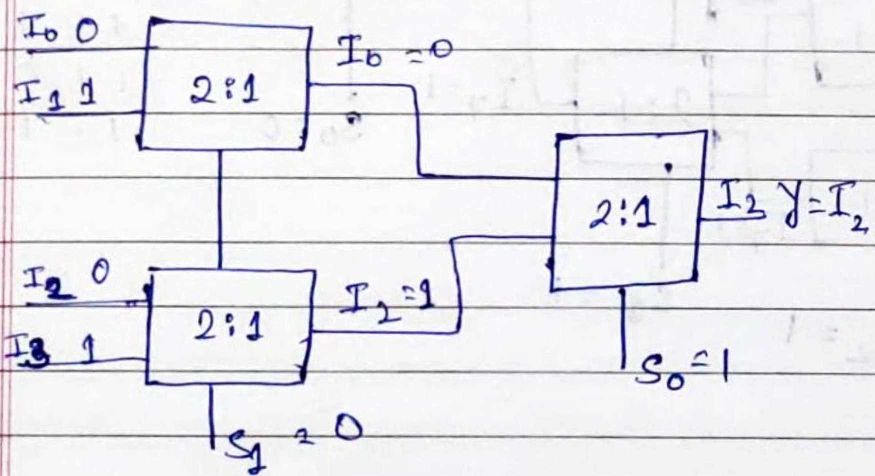
* Higher order mux designing using lower order mux

Q Design 4:1 mux using 2:1 mux

4:1 mux = 2 S.L & 4 I/P's
2:1 mux = 1 S.L & 2 I/P'S

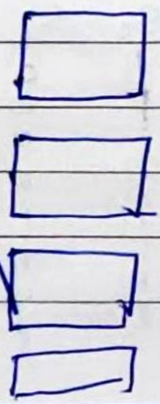
=> $4/2 = 2/2 = 1$



S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

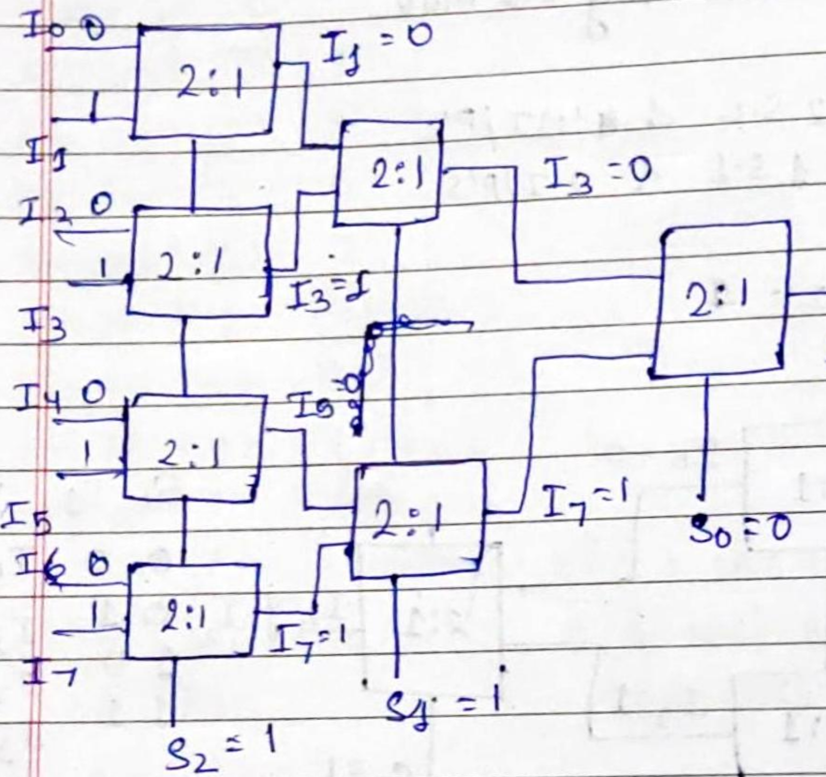
~~Q Design 8:1 mux using 2:1 mux~~

~~$8/2 = 4$~~



Q Design 8:1 mux using 2:1 mux

$8/2 = 4/2 = 2/2 = 1$



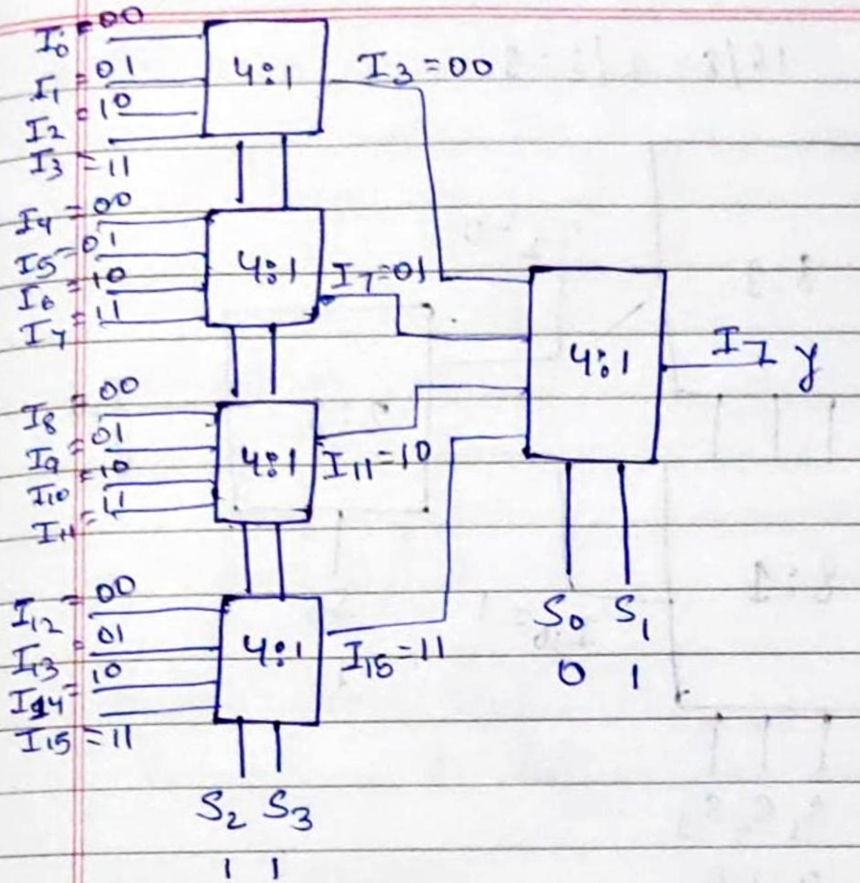
S_0	S_1	S_2	y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

Q Design 16:1 using 4:1

$\frac{16}{4} = \frac{4}{4} = 1$

S_0	S_1	S_2	S_3	y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7

S_0	S_1	S_2	S_3	Y
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}


I0 = 00
I1 = 01
I2 = 10
I3 = 11
I4 = 00
I5 = 01
I6 = 10
I7 = 11
I8 = 00
I9 = 01
I10 = 10
I11 = 11
I12 = 00
I13 = 01
I14 = 10
I15 = 11
4:1
4:1
4:1
4:1
4:1
I3 = 00
I7 = 01
I11 = 10
I15 = 11
I7 y
S0 S1
0 1
S2 S3
1 1

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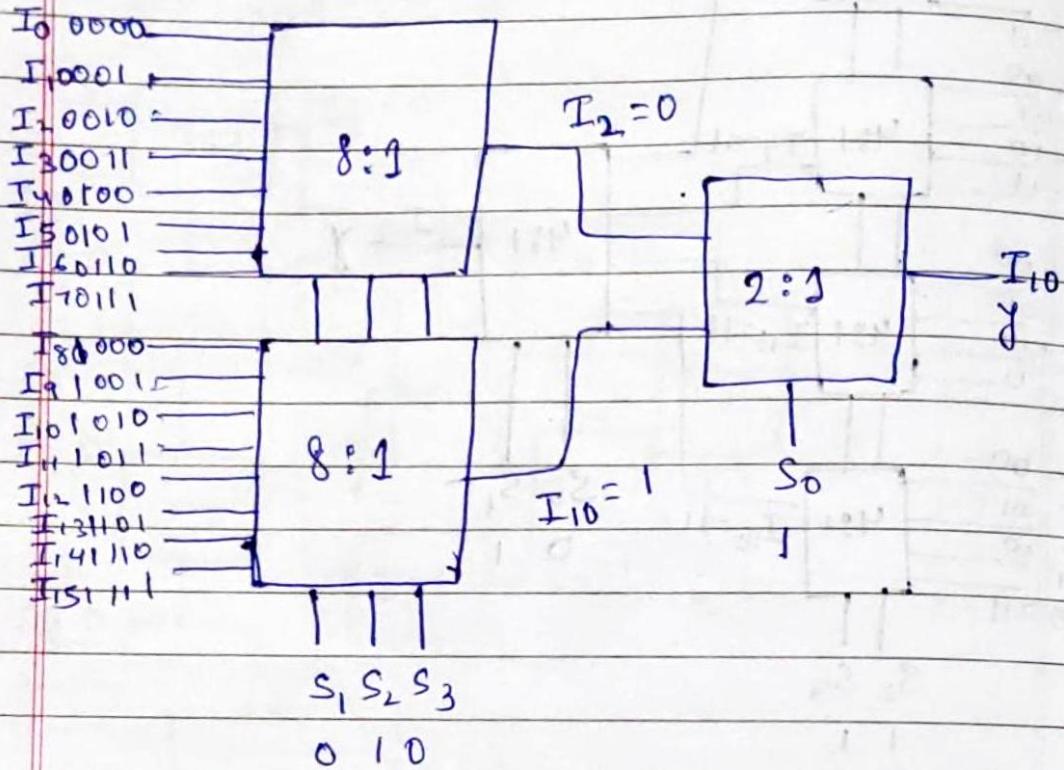
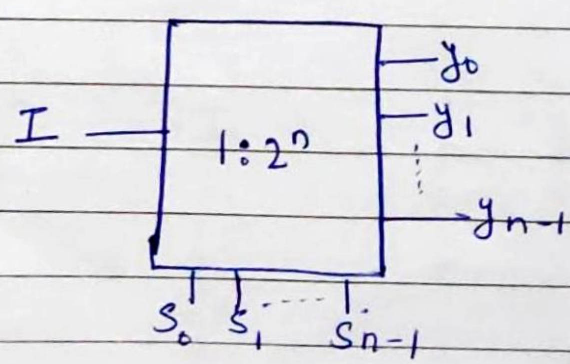
Q 16:1 → 8:1 $\quad$ 16/8 = 2/2 = 1



Encoder → many inputs - many output (To be continued)

Demultiplexer (Demux) → one input - many outputs

$1:2^n$ → no. of select lines



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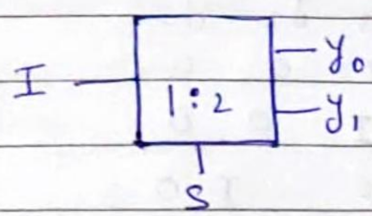
* 1:2 Demux



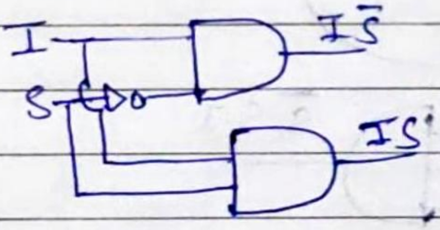
Truth table :-

S	y_0	y_1
0	I	0
1	0	I

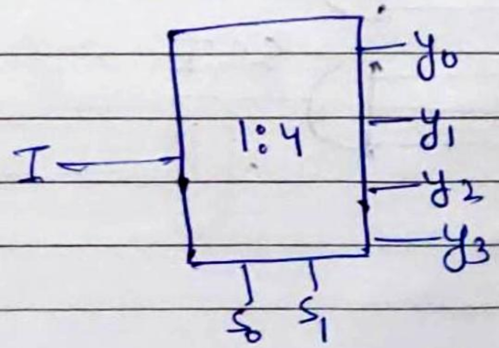
Boolean Expression :-

$y_0 = I\bar{S}$, $y_1 = IS$

Implementation:-



* 1:4 Demux



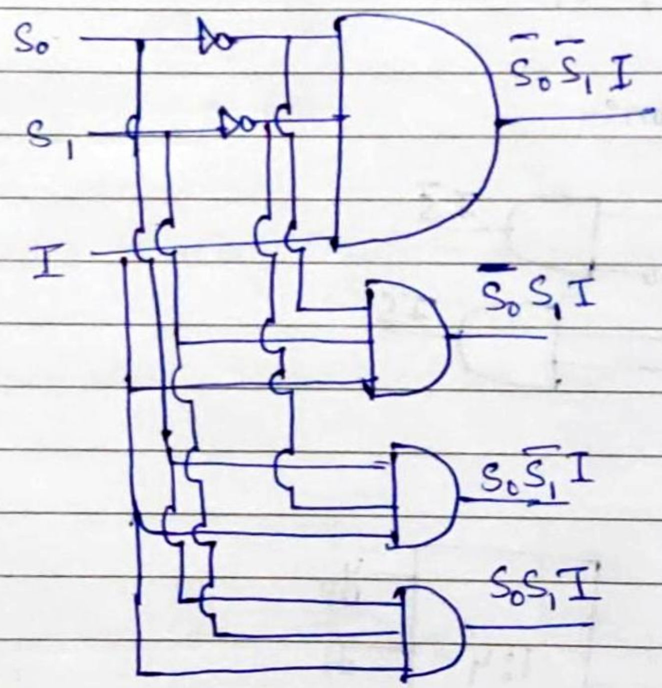
Truth-table :-

S_0	S_1	y_0	y_1	y_2	y_3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

Boolean Expression :-

$y_0 = \bar{S}_0 \bar{S}_1 I$, $y_1 = \bar{S}_0 S_1 I$, $y_2 = S_0 \bar{S}_1 I$, $y_3 = S_0 S_1 I$

Implementation :-

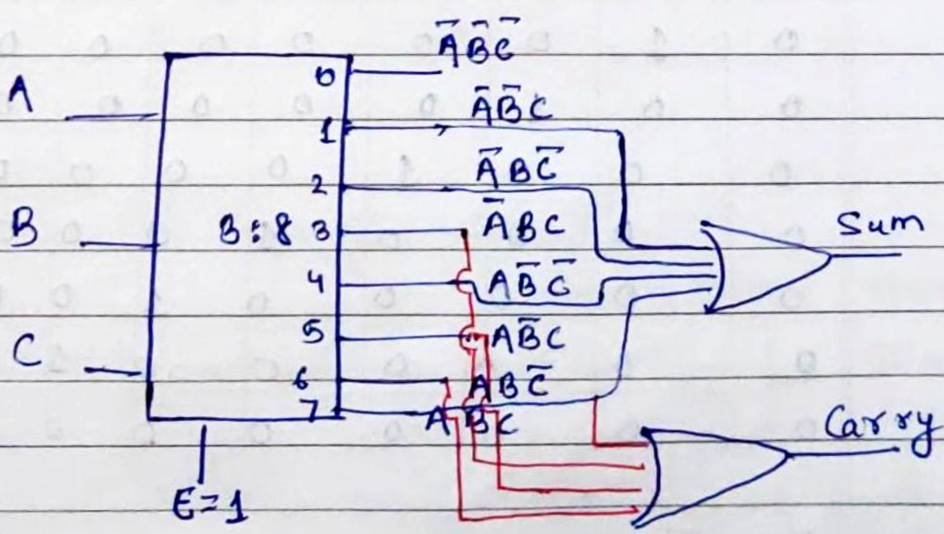


Q. Implement full adder using decoder (if not mentioned the default decoder to be used is 3:8)

Truth-table :-

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum $= \Sigma m(1,2,4,7)$ & Carry $= \Sigma m(3,5,6,7)$



Q. $\bar{A}B + BC + \bar{A}C$

$\bar{A}B(C+\bar{C}) + (A+\bar{A})BC + \bar{A}(B+\bar{B})C$

$\bar{A}BC + \bar{A}B\bar{C} + ABC + \bar{A}BC + \bar{A}BC + \bar{A}\bar{B}C$

$\underset{011}{\bar{A}BC} + \underset{010}{\bar{A}B\bar{C}} + \underset{111}{ABC} + \underset{001}{\bar{A}\bar{B}C}$

$f(A,B,C) = \Sigma m(1, 2, 3, 7)$

Encoder → Many I/P's → Many O/P's

$2^n \rightarrow n$

$2^n : n$

Q. Octal to binary convertor (8:3) encoder

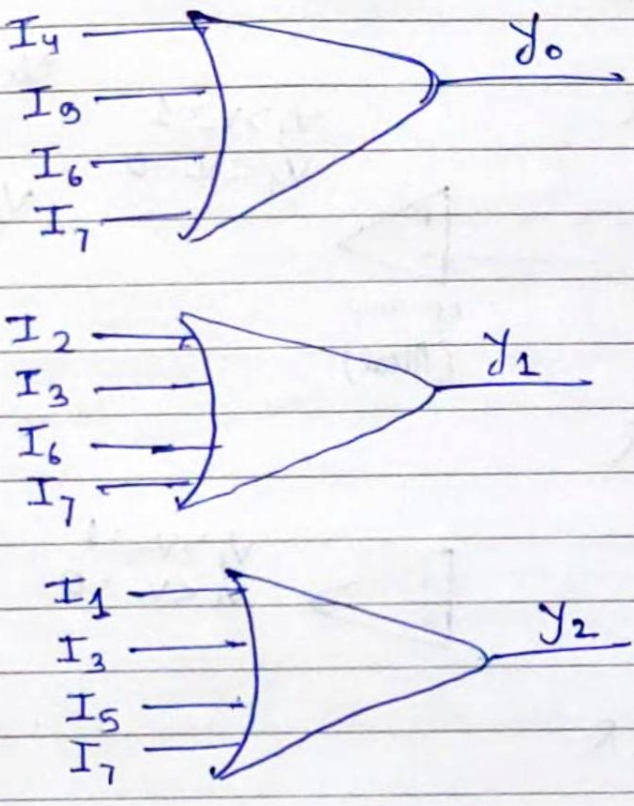
Truth-table :-

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_0	Y_1	Y_2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$Y_0 = I_4 + I_5 + I_6 + I_7$

$y_1 = I_2 + I_3 + I_6 + I_7$
$y_2 = I_1 + I_3 + I_5 + I_7$

Implementation



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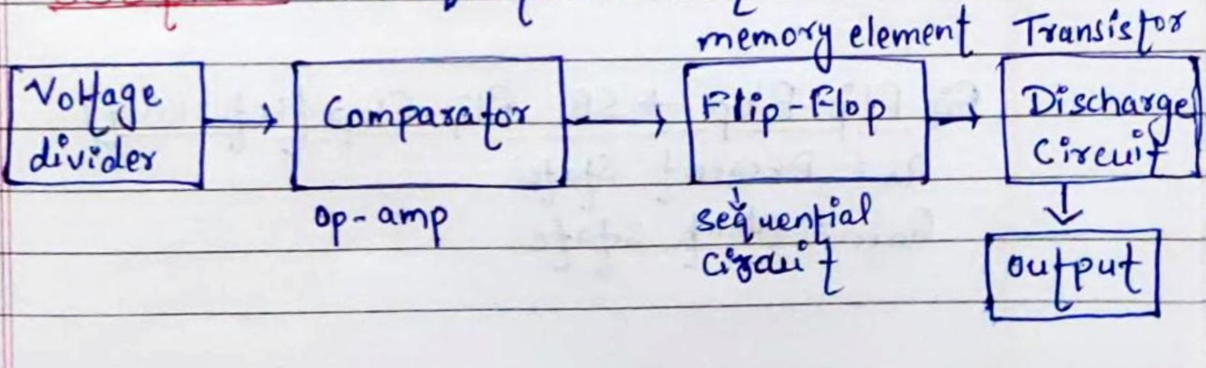
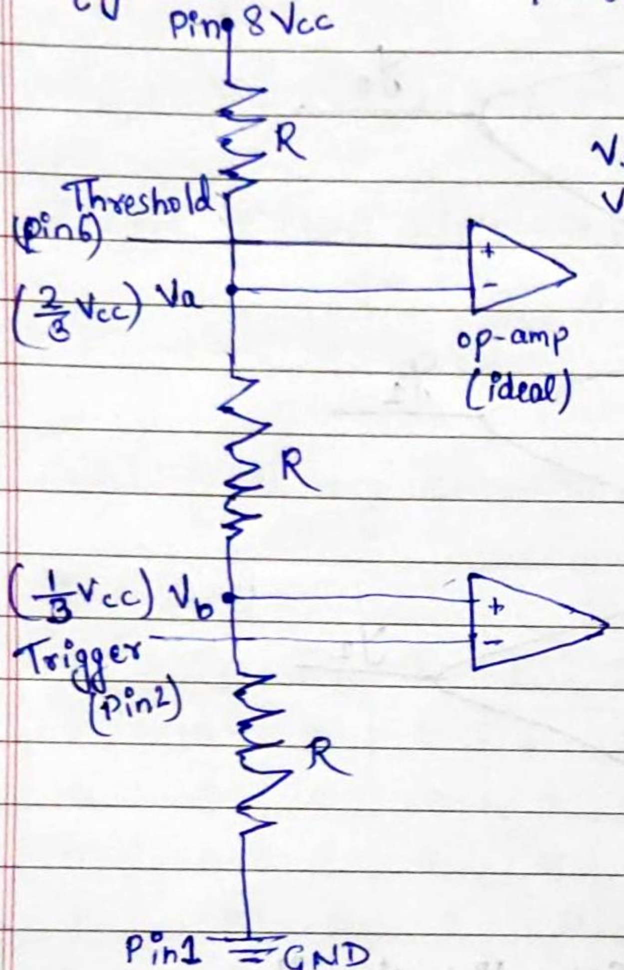
555 timer:- (Part-2) → Sequential circuit



555 timer is a 8 pin IC.
~~Vcc~~ Vcc Supply can varry from 4.5 V to 15 V

Voltage Divider and Comparator:-



$V_+ > V_- = 1$
$V_+ < V_- = 0$

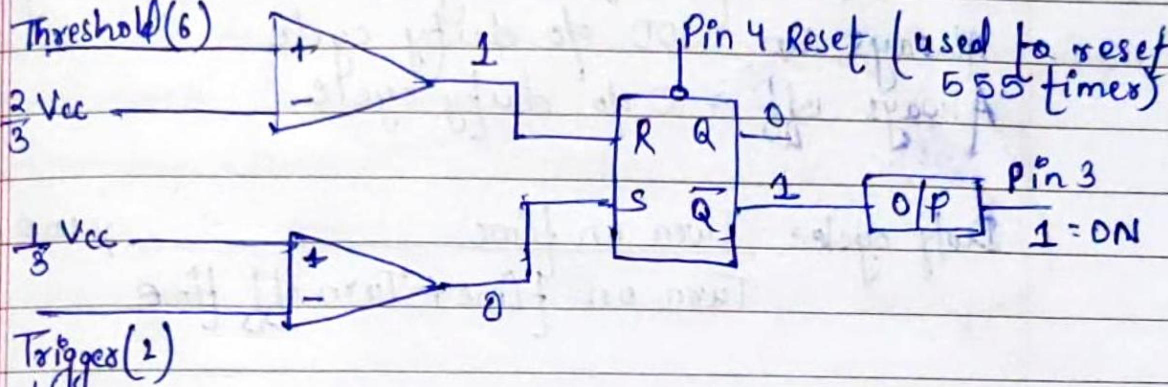
$V_a = \frac{2R \times V_{cc}}{2R + R} = \frac{2}{3}V_{cc}$

$V_b = \frac{R \times V_{cc}}{2R + R} = \frac{1}{3}V_{cc}$

$V_+ > V_- = 1$
$V_+ < V_- = 0$

Flip-Flop → SR flip Flop (set-Reset)
Q_n = Present State
Q_{n+1} = Next State

S	R	Qn	Qn+1
0	0	0/1	0/1
0	1	0/1	0
1	0	0/1	1
1	1	0/1	Invalid

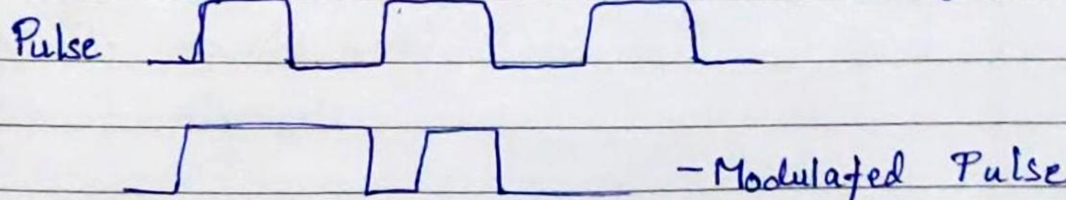


↓
Normally remains of Vcc

Using the 2nd & 6th pin we are controlling the O/P voltage.

(Part-1)

PWM (Pulse width Modulation) → Used in control circuit
↓
Square wave

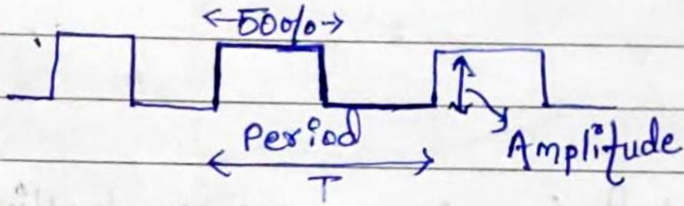


Controls $\boxed{\text{memory element}}$ → Flip-Flop / Latches
↳ Pulse width → clock → square wave

Duty-cycle :- The percentage of time in which the pwm signal remains high (on time)

Always on = 100 % duty cycle
Always off = 0 % duty cycle

$$\text{Duty cycle} = \frac{\text{Turn on time}}{\text{Turn on time} + \text{Turn off time}} \times 100$$



$$\boxed{f = 1/T}$$

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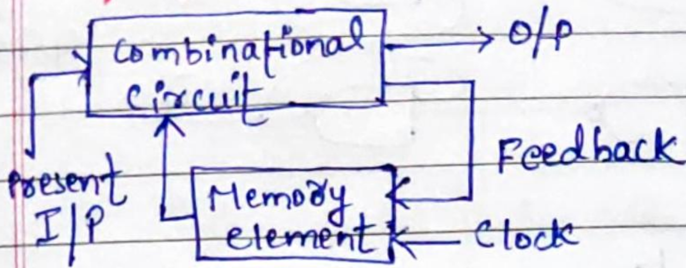
Sequential Circuits



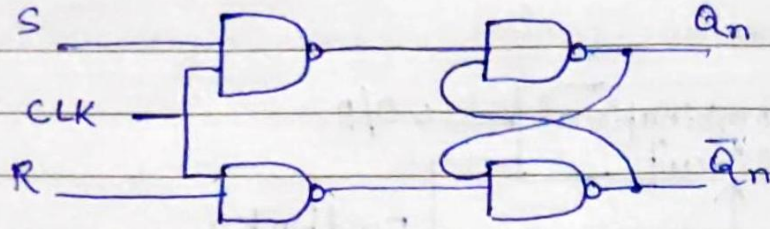
- Output depends on present & past/previous inputs
- Feedback is present
- Memory element is present
- Clock is present.
- ~~Flip/flop~~ Flip-flop's, counters, shift resistors.

Flip-flops :-

* It is a basic memory element which stores only one bit either 0 or 1.
* In flip-flop there are two outputs which are compliments of each other.
* Bistable multivibrator :- because it has only two stable states either 0 or 1.
* frequency divider, lifts, traffic light system.

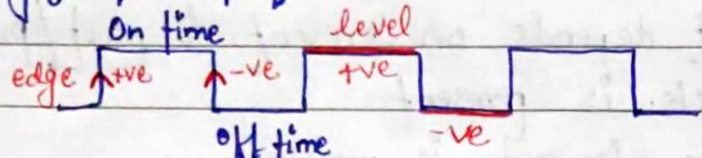
SR flip-flops (Set-Reset)

Circuit diagram:-



Q_n = Present State
Q_{n+1} = Next State

CLK:- Digital pulse / Square wave



→ 50 % duty cycle

CLK
- Edge
  - +ve edge (1)
  - -ve edge (0)
- Level
  - +ve level (1)
  - -ve level (0)

Edge allows less number of changes than level reason being it is one for small interval of time.

Memory element
- Flip-flop
  ↓
  edge of the Clock
  |
  Small interval.
- Latch
  ↓
  Level of the clock

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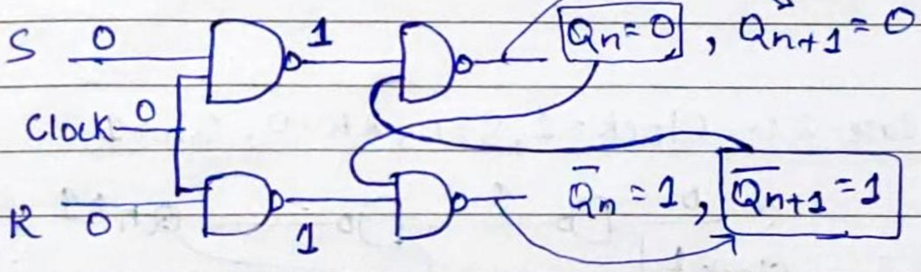
SR Flip-flop

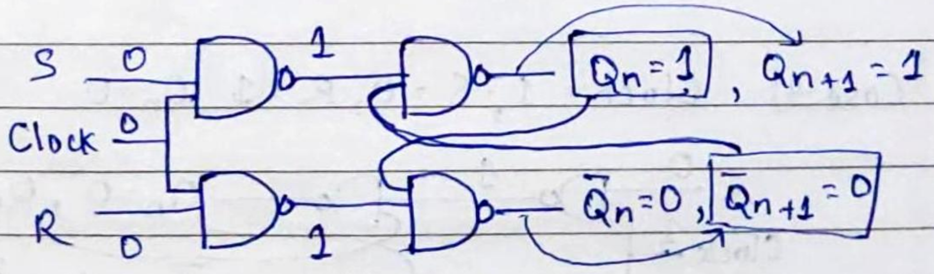
Truth-table :-

Clock	S	R	Q_{n+1}
0	0	0	Q_n
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n

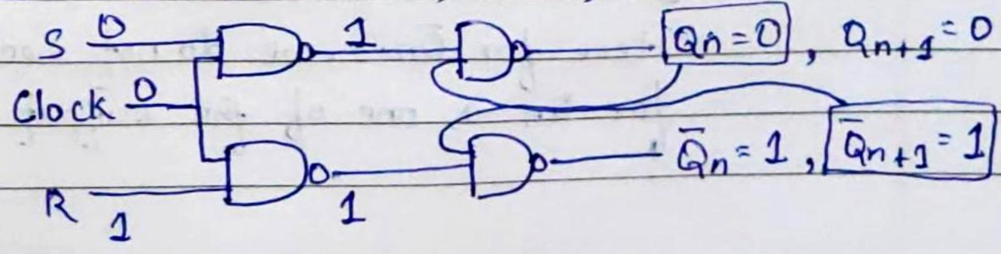
Case-1 Clock = 0 , S = 0, R = 0, Q_n = 0



Case - 2 Clock = 0, S = 0, R = 0 , Q_n = 1

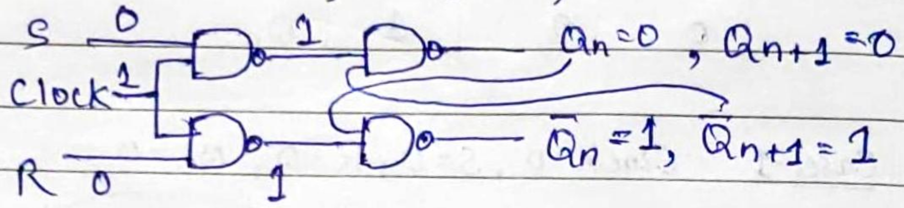


Case-3 Clock = 0 , S = 0, R = 1 , Q_n = 0

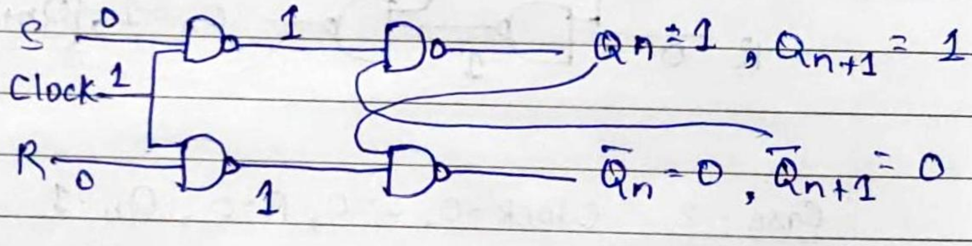


Clock	S	R	Q_{n+1}
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

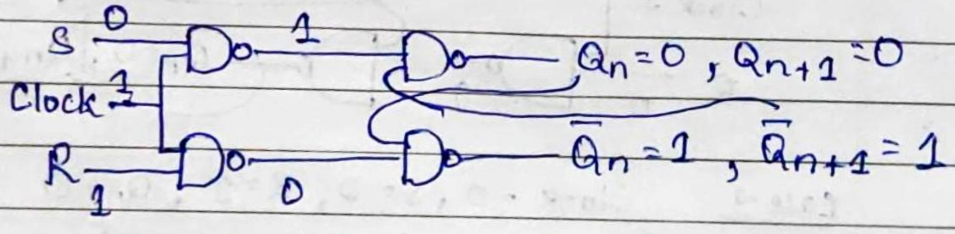
<u>Case-1</u> :- Clock = 1, S = 0, R = 0, $Q_n = 0$



<u>Case-2</u> :- Clock = 1, S = 0, R = 0, $Q_n = 1$

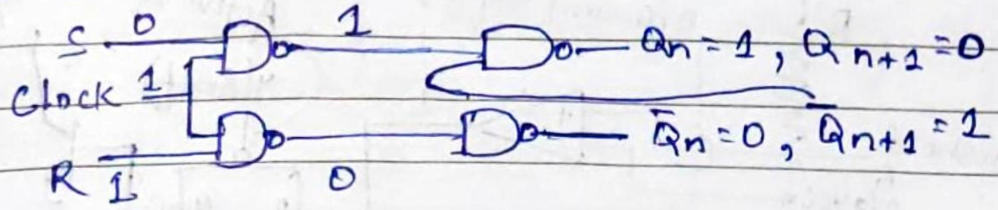


<u>Case-3</u> :- Clock = 1, S = 0, R = 1, $Q_n = 0$

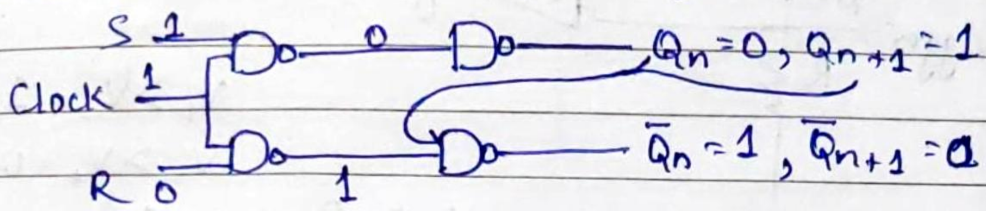


Here for $\bar{Q}_{n+1}$, we do not need to wait for Q_n as one of the output is 0

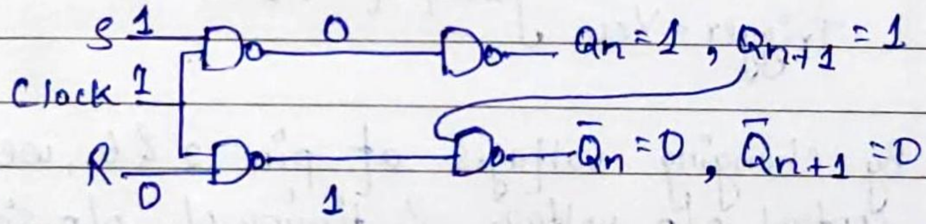
Case 4:- Clock = 1, S = 0, R = 1, $Q_n = 1$



Case 5:- Clock = 1, S = 1, R = 0, $Q_n = 0$



Case 6:- Clock = 1, S = 1, R = 0, $Q_n = 1$



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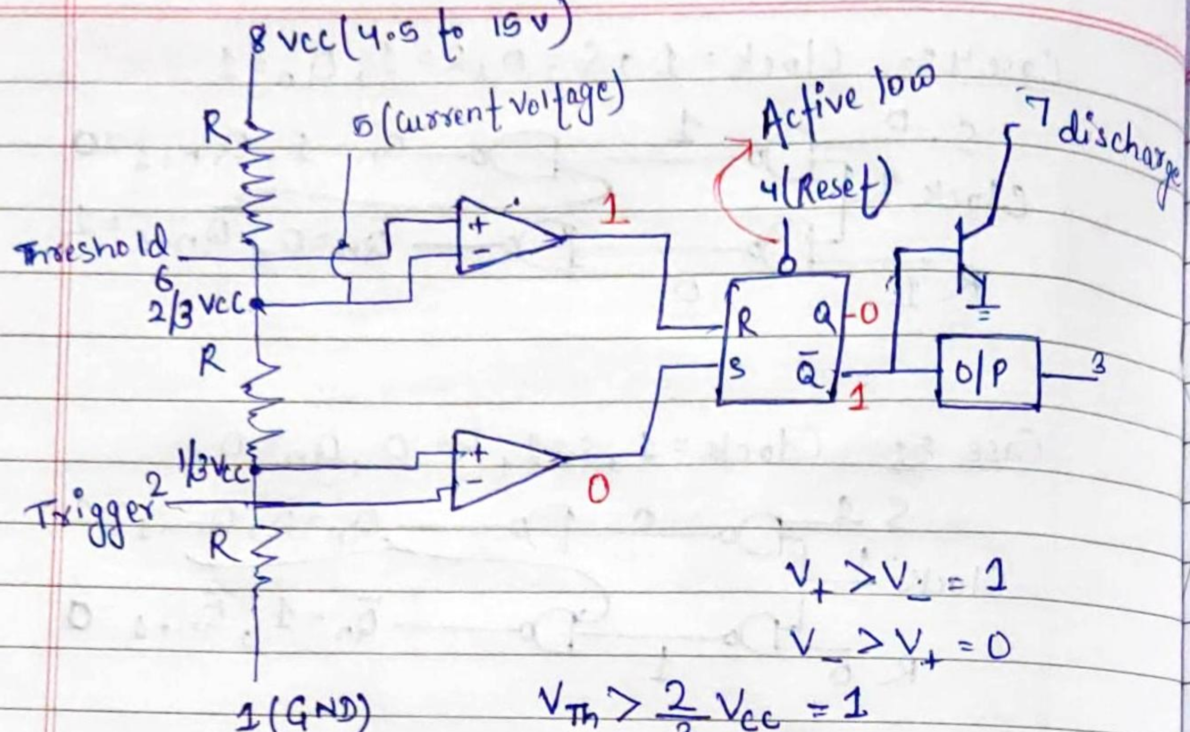
Pulse-width modulation (555 timer)



$V_+ > V_- = 1$

$V_- > V_+ = 0$

$V_{Th} > \frac{2}{3} V_{cc} = 1$

$\frac{1}{3} V_{cc} > V_{Tr} = 1$

$\left.\begin{array}{l}\text{Threshold} = V_{cc} \\ \text{Trigger} = V_{cc}\end{array}\right\} \text{Output} = 1 \& 0$

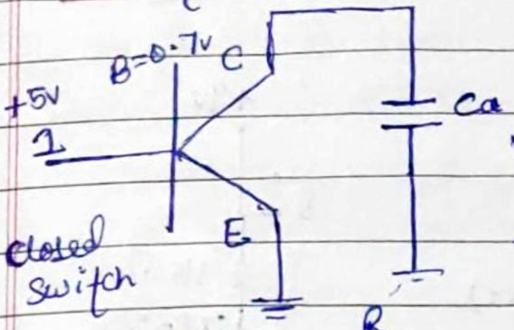
* By changing voltages at pin 2 & 6, we can ~~change~~ control o/p voltage & timing of o/p signal.

Q How to change voltages at threshold & trigger pin?

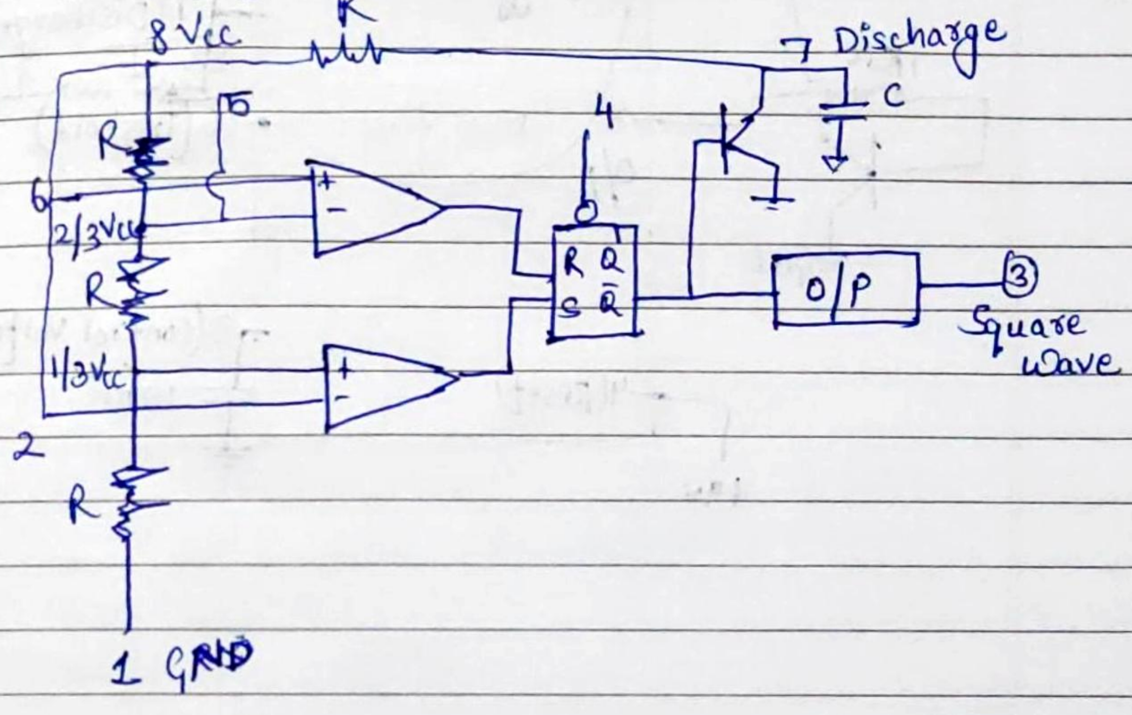
→ By connecting ~~external~~ ~~rest~~ external resistor & capacitor b/w the threshold, trigger & discharge pin through the supply voltage.

Transistors:-

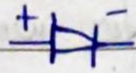
Transistor working as switch

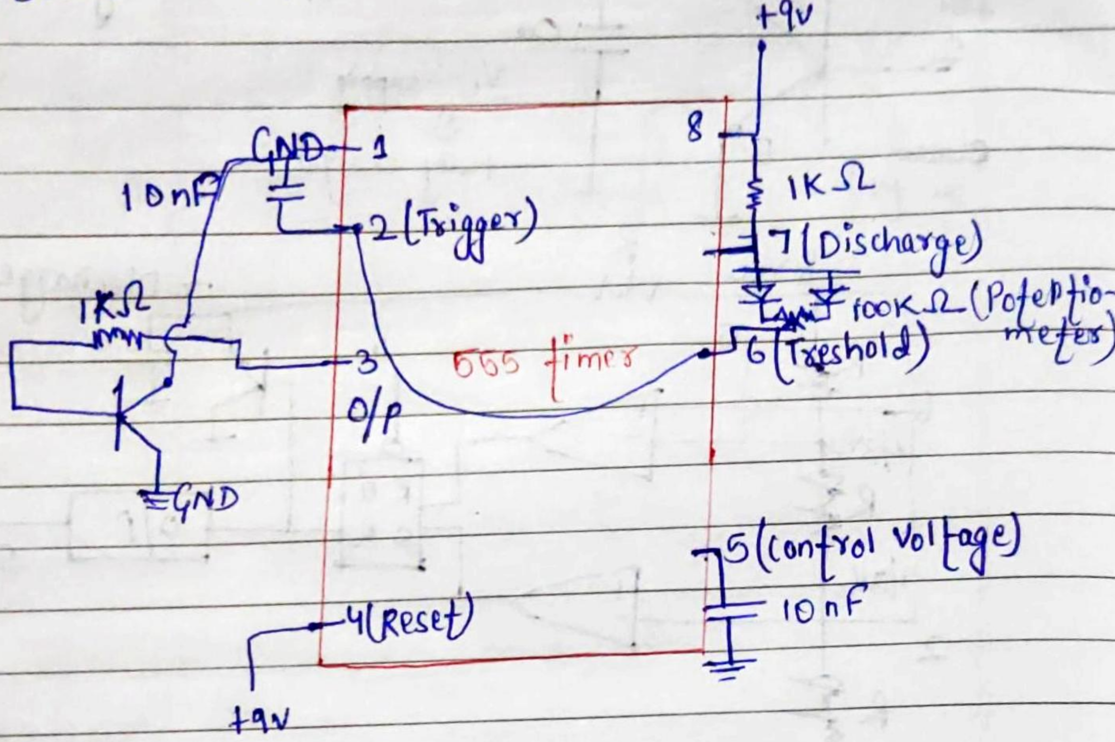


$V_c = V_{supply}$
⇓
fully charged



Tinkercad Circuit

Diode → 



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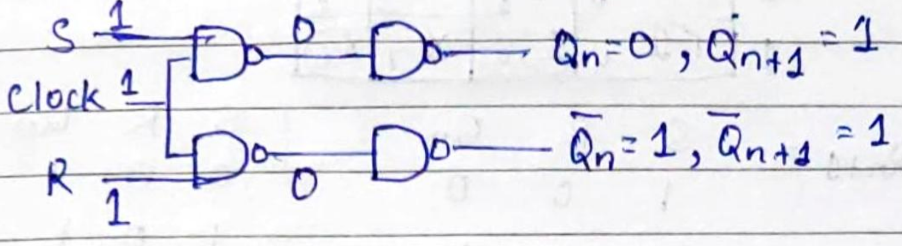
S-R Flip-flop

Truth-table when clock = 1

Case-7 :- Clock = 1, S = 1, R = 1, $Q_n = 0$



Truth-table :-

Clock	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	x. ~~Invalid~~

Characteristic table :-

Clock	S	R	Q_n	Q_{n+1}	
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	0	2
1	0	1	1	0	3
1	1	0	0	1	4
1	1	0	1	1	5
1	1	1	0	x	6
1	1	1	1	x	7

Characteristic equation:-

S \ RQ_n	00	01	11	10
0	₀	1 ₁	₃	₂
1	1 ₄	1 ₅	X ₇	X ₆

	S	R	Q_n
$Q_{n+1} =$	1	0	0
	1	0	1
	1	1	1
	1	1	0
	S	x	x

S	R	Q_n
0	0	1
1	0	1
x	$\bar{R}$	Q_n

$= S + \bar{R}Q_n$

Excitation Table:-

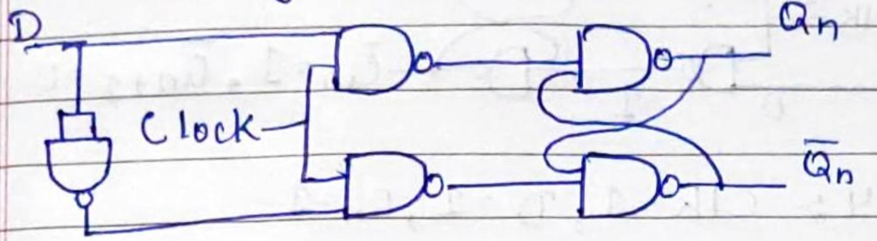
~~Q_n~~	~~Q_{n+1}~~	~~S~~	R
~~0~~	~~0~~	~~0 0~~	0 1
~~0~~	~~1~~		
~~1~~	~~0~~		
~~1~~	~~1~~		

Q_n	Q_{n+1}	S R
0	0	0 0 0X
		0 1
0	1	1 0
1	0	0 1
1	1	0 0 X0
		1 0

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop (Data flip-flop)

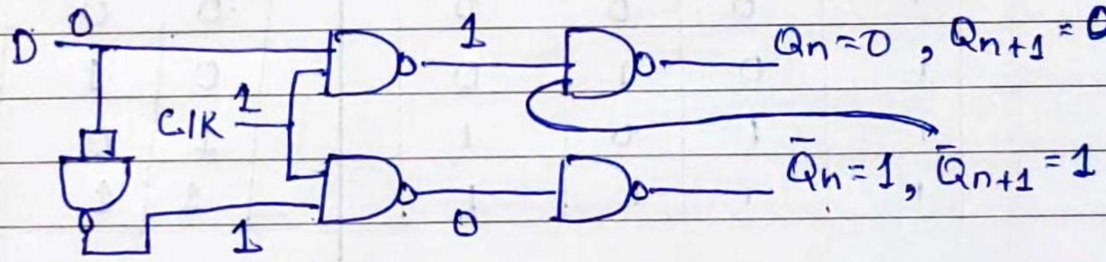
Circuit diagram:-



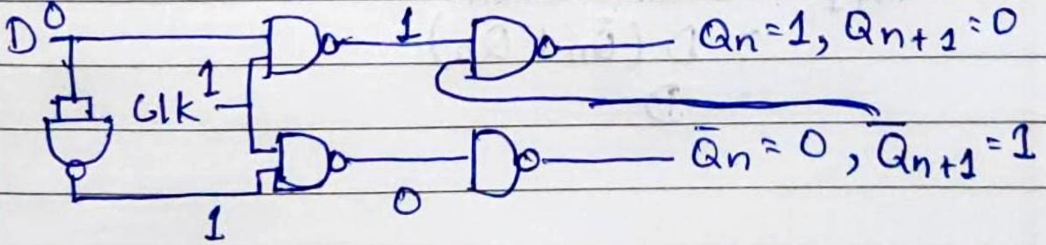
Truth Table :-

Clock	D	Q_{n+1}
1	0	D
1	1	D

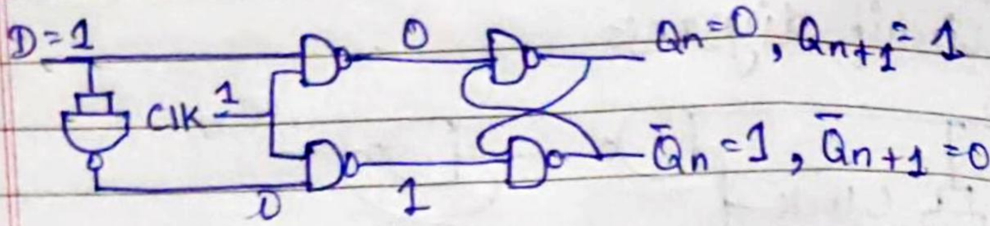
Case 1 :- $Clk = 1, D = 0, Q_n = 0$



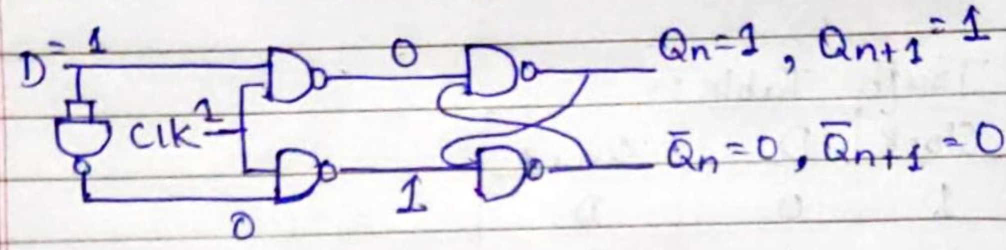
Case 2 :- $Clk = 1, D = 0, Q_n = 1$



Case 3 :- $Clk = 1, D = 1, Q_n = 0$



Case 4 :- $Clk = 1; D = 1, Q_n = 1$



Characteristic Table:-

Clk	D	Q_n	Q_{n+1}
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Excitation Table:-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic equation :-

$$Q_{n+1} = D\bar{Q}_n + DQ_n$$
$$= D(\bar{Q}_n + Q_n)$$
$$= D$$

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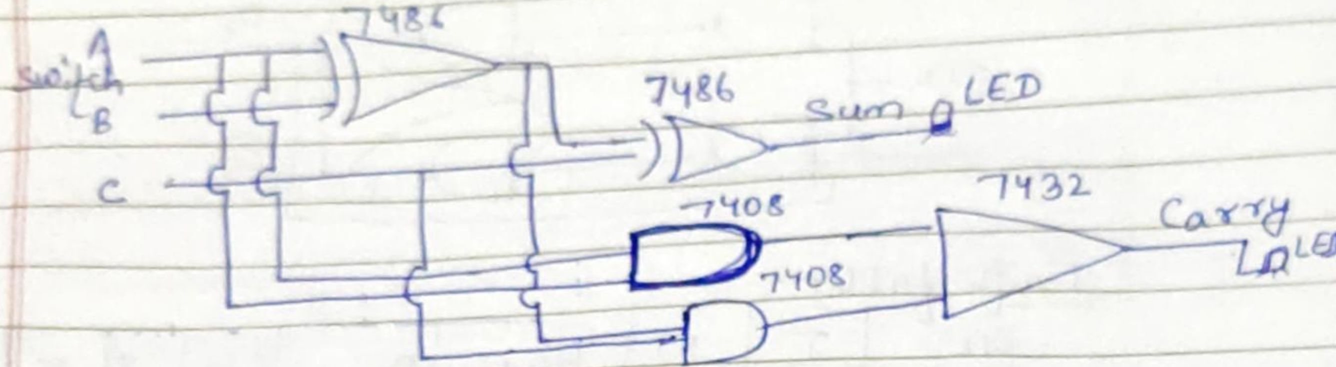
Make full-adder on tinkercad.

Sum = $A \oplus B \oplus C$

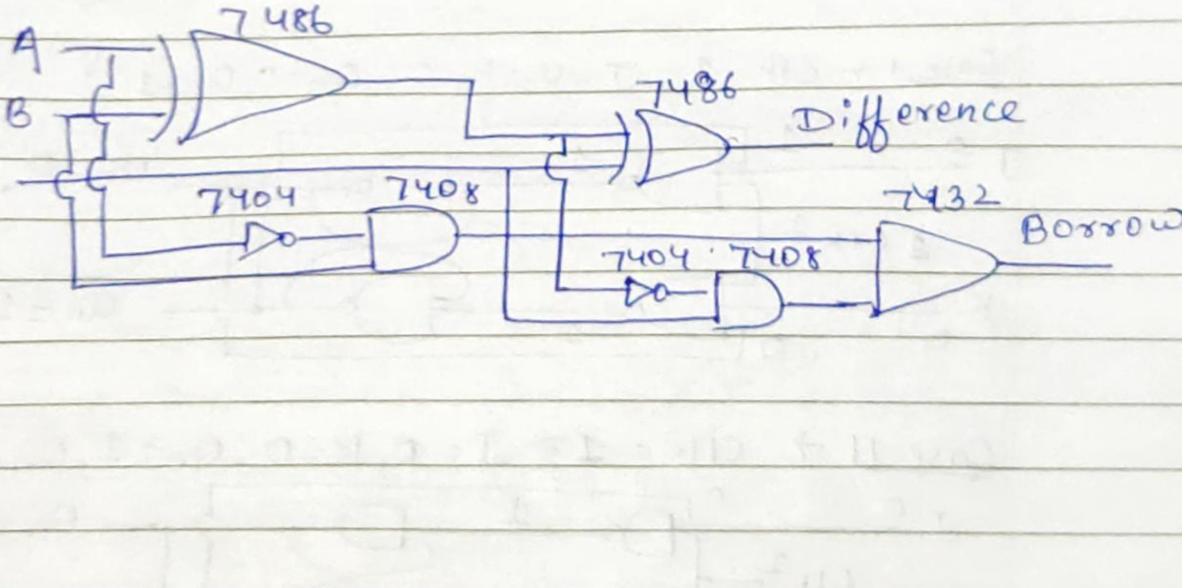
Carry = $AB + (A \oplus B) C$



Make full-subtractor on tinkercad

Difference = $A \oplus B \oplus C$

Borrow = $\bar{A}B + C(\overline{A \oplus B})$



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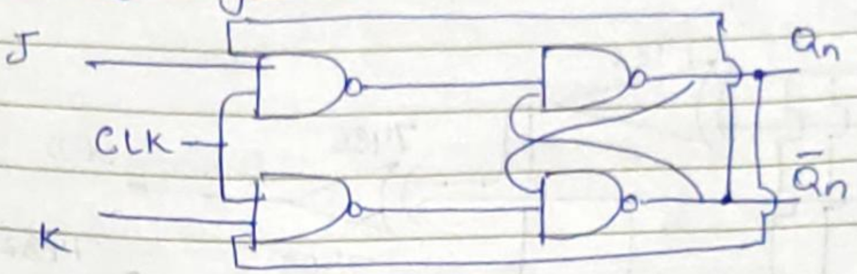
J-K Flip flop :- (Jack Kilby)

Circuit diagram-

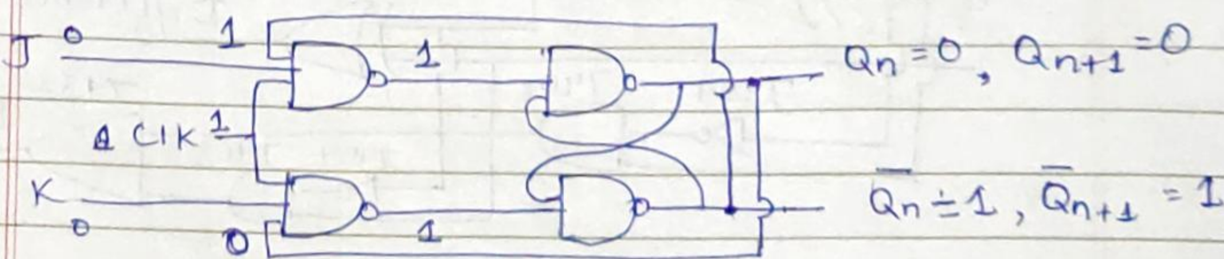


Truth-table:-

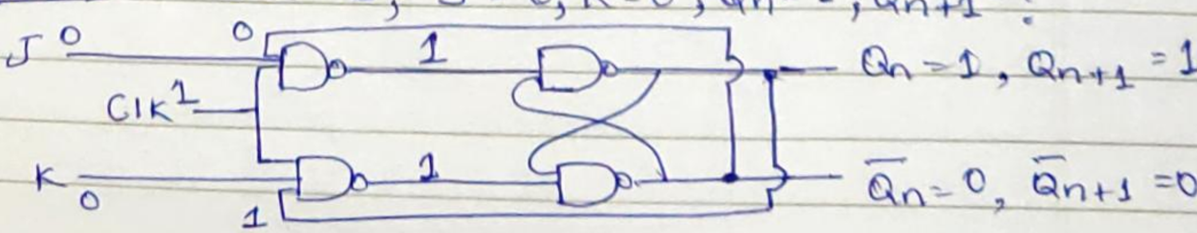
Clk	J	K	Q_{n+1}	Q_n
1	0	0	0/1	0/1
1	0	1	0	0/1
1	1	0	1	0/1
1	1	1	1/0	0/1 (Toggle)

Clk	J	K	Q_{n+1}
0	x	x	Q_n

Case I → Clk = 1, J = 0, K = 0, $Q_n = 0$, $Q_{n+1} = ?$

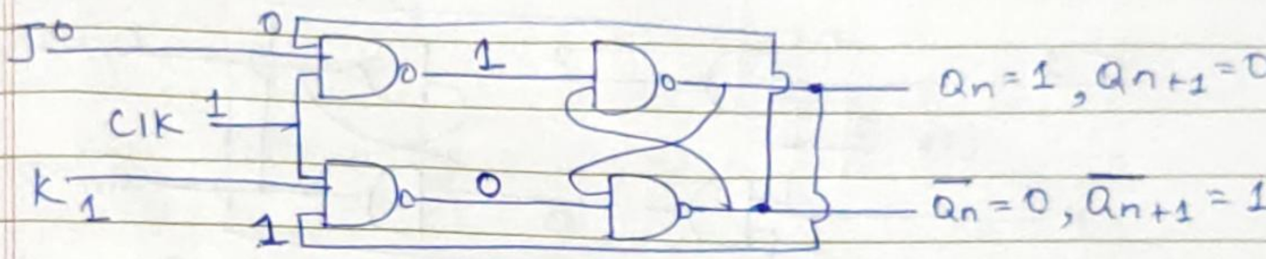


Case II → Clk = 1, J = 0, K = 0, $Q_n = 1$, $Q_{n+1} = ?$



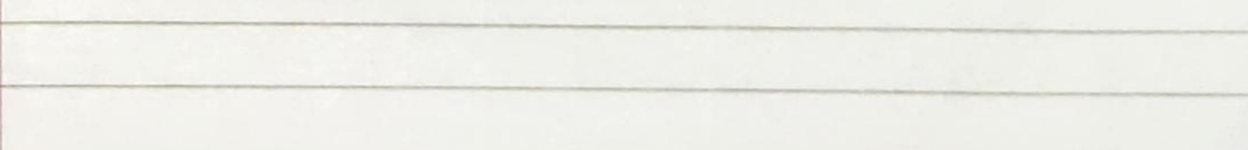
Case III → Clk = 1, J = 0, K = 1, Q_n = 0, Q_{n+1} = ?

Case IV → Clk = 1, J = 0, K = 1, Q_n = 1, Q_{n+1} = ?

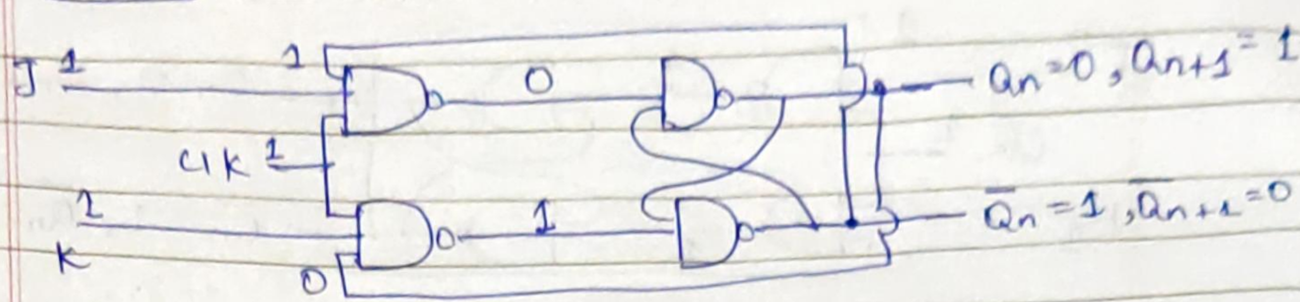


Case V → Clk = 1, J = ~~0~~1, K = 0, Q_n = 0, Q_{n+1} = ?

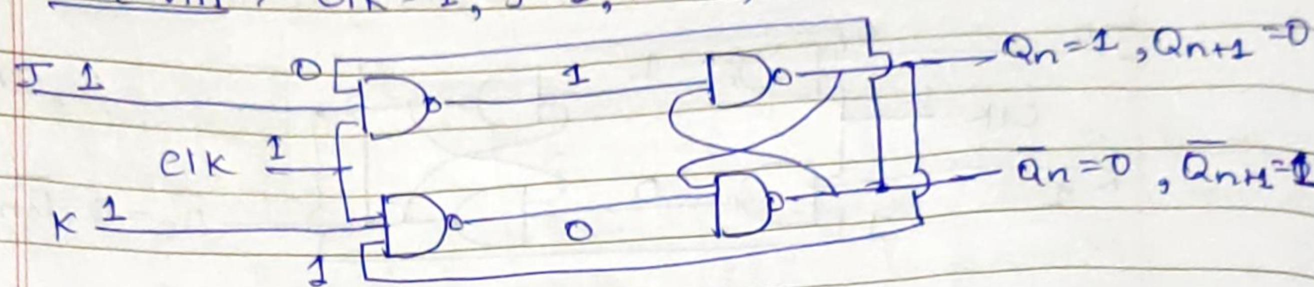
Case VI → Clk = 1, J = 1, K = 0, Q_n = 1, Q_{n+1} = ?



Case VII → $Clk = 1$, $J = 1$, $K = 1$, $Q_n = 0$, $Q_{n+1} = ?$



Case VIII → $Clk = 1$, $J = 1$, $K = 1$, $Q_n = 1 = Q_{n+1} = ?$



Characteristic table-

Clk	J	K	Q_n	Q_{n+1}
1	0	0	0	0
	0	0	1	1
1	0	1	0	0
	0	1	1	0
1	1	0	0	1
	1	0	1	1
1	1	1	0	1
	1	1	1	0

Characteristic eqn:

J \ KQ_n	00	01	11	10
0	[0]	1 [1]	[3]	[2]
1	1 [4]	1 [5]	[7]	1 [6]

J	K	Q_n
0	0	1
1	0	1
x	$\bar{K}$	Q_n

J	K	Q_n
1	0	0
1	1	0
J	x	$\bar{Q}_n$

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Excitation table-

Q_n	Q_{n+1}	J	K		
0	0	0	0	0	X
		0	1		
0	1	1	0	1	X
		1	1		
1	0	0	1	X	0
		1	1		
1	1	0	0	X	1
		1	0		

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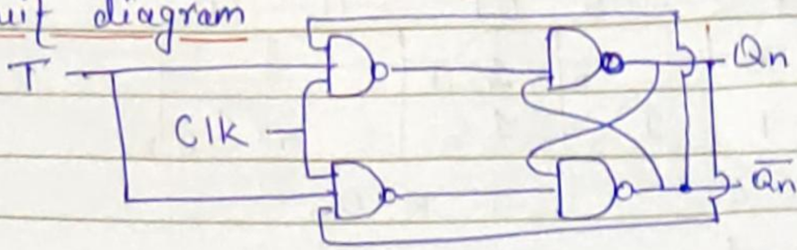
T Flip-flop (Toggle flip-flop)

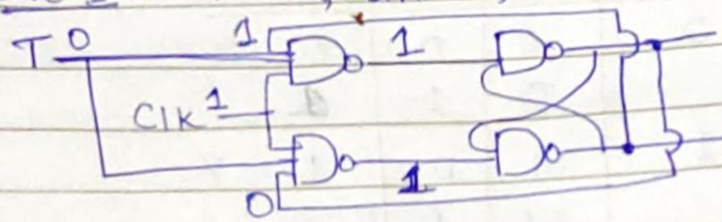
Circuit diagram



Truth-table.

Clk	T	Q_{n+1}
1	0	Q_n
1	1	$\bar{Q}_n$

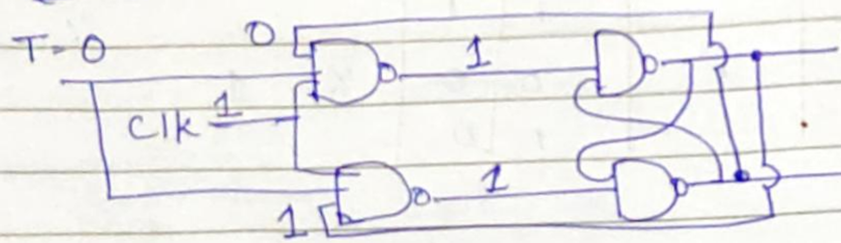
Case I :- $T = 0$, $Q_n = 0$, $Q_{n+1} = ?$, $Clk = 1$



$Q_n = 0$, $Q_{n+1} = 0$

$\bar{Q}_n = 1$, $\bar{Q}_{n+1} = 1$

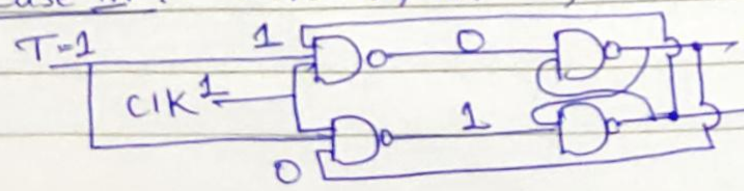
Case II :- $Clk = 1$, $Q_n = 1$, $T = 0$, $Q_{n+1} = ?$



$Q_n = 1$, $Q_{n+1} = 1$

$\bar{Q}_n = 0$, $\bar{Q}_{n+1} = 0$

Case III :- $Clk = 1$, $Q_n = 0$, $T = 1$, $Q_{n+1} = ?$



$Q_n = 0$, $Q_{n+1} = 1$

$\bar{Q}_n = 1$, $\bar{Q}_{n+1} = 0$

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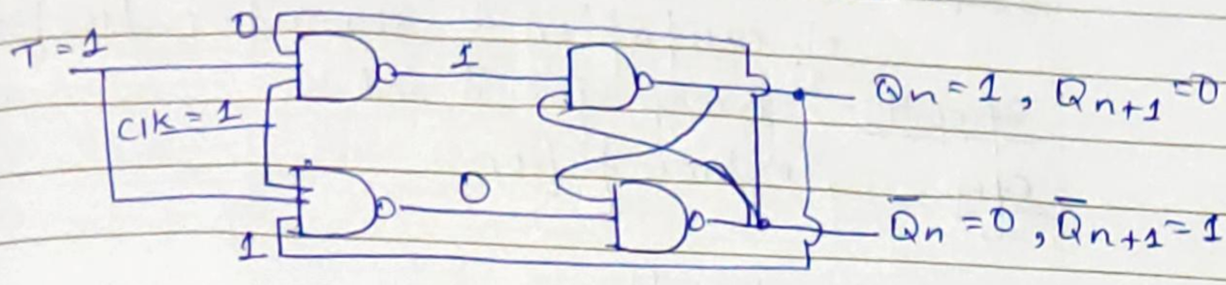
Case IV :- $Clk = 1$, $T = 1$, $Q_n = 1$, $Q_{n+1} = ?$



Characteristic table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic eqn

$$Q_{n+1} = \bar{T} Q_n + T \bar{Q}_n$$
$$= T \oplus Q_n$$

Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Flip-flop conversions :-

Q Convert J-K flip-flop in D flip-flop ?

Step 1 :- Given flip-flop i.e., JK, Required flip-flop 'D'

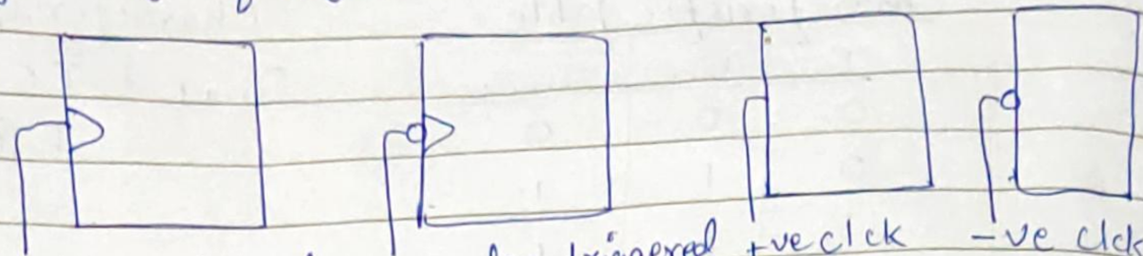
Step 2 :- Excitation table of given flip-flop and characteristic table of required flip-flop

<u>Step 3</u>:- Make conversion table with the combination of excitation & characteristic table

<u>Step 4</u>:- Kmap for J and K

<u>Step 5</u> :- Implementation

<u>Symbols for flip-flop</u>



+ve edge triggered clck   -ve edge triggered clck   +ve clck level   -ve clck level

→ <u>STEP2:-</u>

JK (E.T)

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D (C.T)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Step 3 :-

Conversion table

D	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

Step 4:-

K-Map for J

D \ Q_n	0	1
0	$_0$	X $_1$
1	1 $_2$	X $_3$

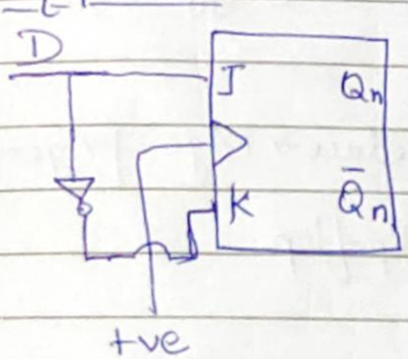
$J = D$

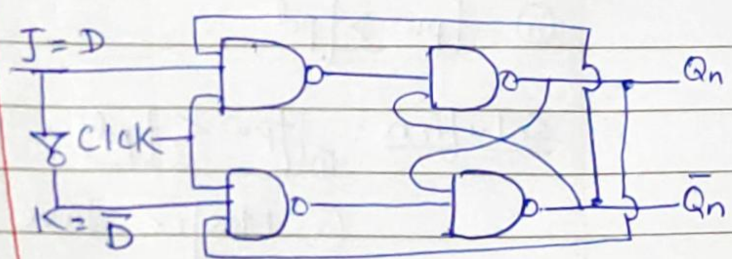
K-Map for K

D \ Q_n	0	1
0	X $_0$	1 $_1$
1	X $_2$	$_3$

$K = \overline{D}$

Step 5:-





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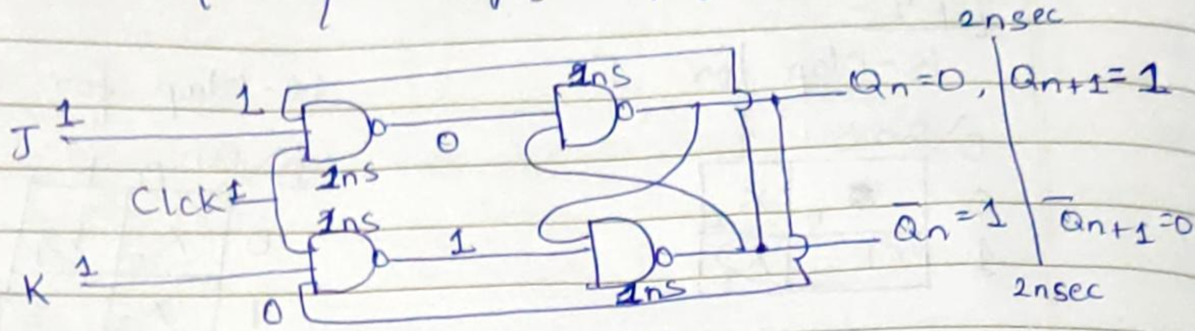
Race around condition

① It occurs in JK flip-flop
when J=1, K=1

② It only occurs with the lvl of the clock is taken

tpw - time period of Pulse width = 10n sec (refrence)
tpd - propagation delay time period = 1n(sec) (refrence)
↳ time taken by the input to reach output.



When race around condition occurs:-

(i) J=1, K=1, Clck = +ve level triggered
(ii) tpw > tpd

Solution :- ① (tpw < tpd) Reduce → edge trigerring
② Master slave flip-flop

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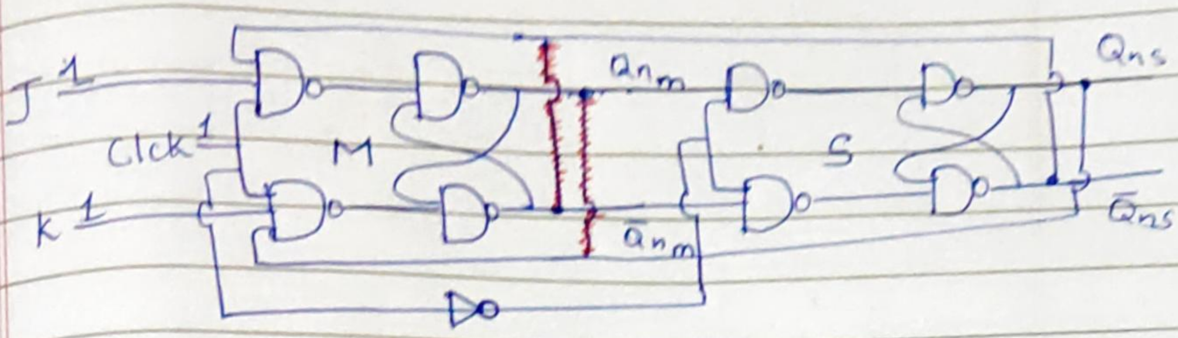
Master-slave flip flop:-



① Final o/p will be given by slave
② Slave follows the master

Master-slave does not stop toggling but help in making the toggling in controlled manner. i.e., output is not changing multiple times.

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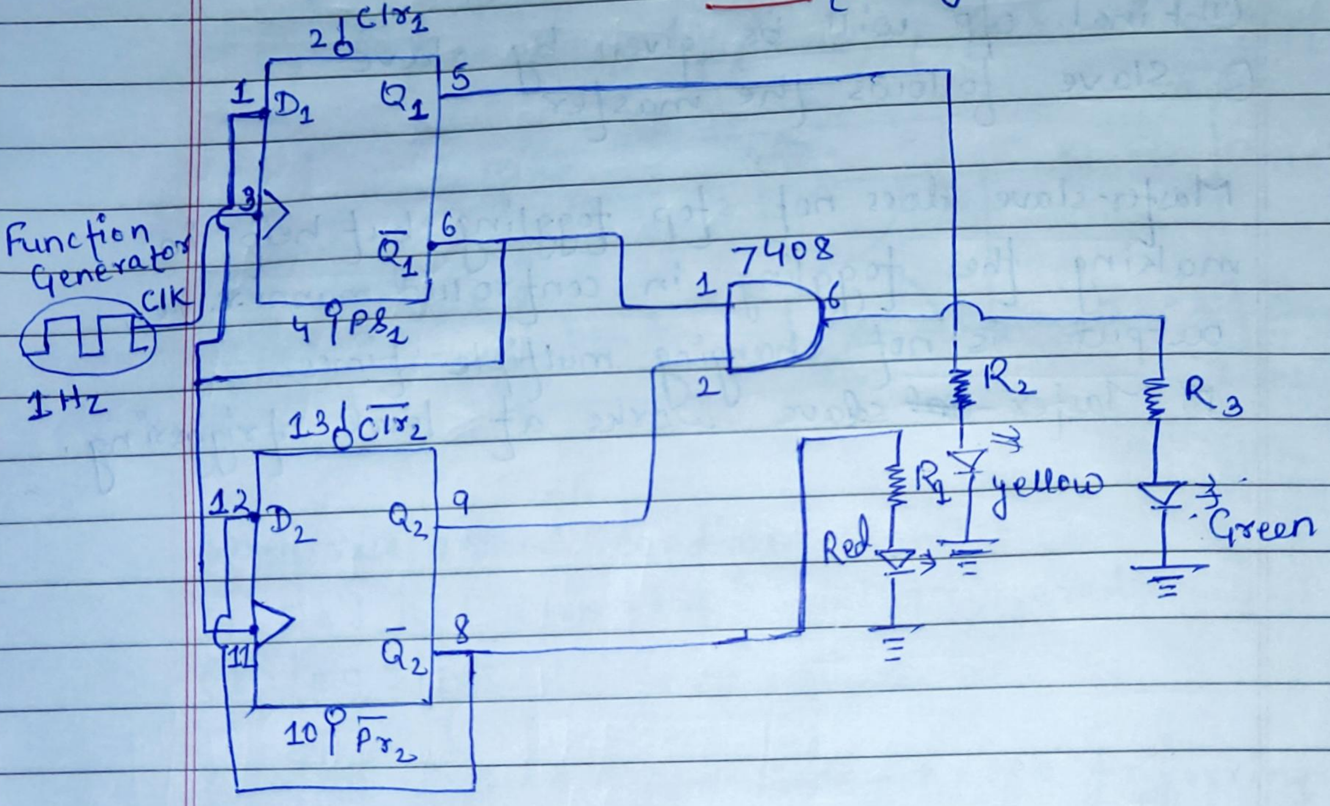
D flip-flop + Traffic light system

IC number for D-flipflop 7474

Truth-table:

D	Q_{n+1}
0	0
1	1

Circuit diagram:-



Step1:- Initially $D_1 = 0$, $D_2 = 0$
Clear, preset = high

If $Q_1 = 1$, ~~red will glow~~ yellow will glow

When $\overline{Q_1} \cdot Q_2$, green will glow

$\overline{Q_2} = 1$, red will glow

Step 2:- 1st positive edge occurs

$D_1 = 0$, , $Q_1 = 0$ (yellow not glowing)

$\bar{Q}_1 = 1$ (clck of 2nd flip-flop)

$D_2 = 0$, $Q_2 = 0$ (Green not glowing)

$\bar{Q}_2 = 1$ (Red will glow)

Step 3:- After 1st positive edge

$D_1 = 1$, $D_2 = 1$

but the changes will not appear on the output as level is going on.

Step 4:- 2nd positive edge occurs

$D_1 = 1$, $Q_1 = 1$ (Yellow will glow)

$\bar{Q}_1 = 0$ (Green will not glow)

$D_2 = \bar{Q}_1 = 0$ (Red will not glow)

Step 5:- After 2^{nd} positive edge

$D_1 = 0$, $D_2 = 1$

Step 6:- 3rd positive edge

$D_1 = 0$, $Q_1 = 0$ (Yellow will not glow)

$\bar{Q}_1 = D_2 = 1$, $Q_2 = 1$ (Green will glow)

$\bar{Q}_2 = 0$ (Red will not glow)